TECHNICAL MANUAL

GENERAL SUPPORT MAINTENANCE MANUAL

TEST SET, SIGNAL DATA CONVERTER AN/AYM-8 (FSN 6625-137-2289)

HEADQUARTERS, DEPARTMENT OF THE ARMY
MAY 1975

WARNING NOTICES

WARNING

Low voltages hazardous to life exist in Test Set, Signal Data Converter AN/AYM-8 when it is connected to external primary power sources. The following voltages exist at the connectors and junctions specified:

1ASJ1/2W8P	115 Vac, 28 Vdc
1A3J4	26 Vac

WARNING

High voltages hazardous to life exist within Test Set, Signal Data Con**verter AN/AYM-8** when it is connected to the unit it is testing. A voltage of approximately +525 Vdc exists in connector 1A3J2 and in the area of the DISPLAY cathode ray tube.

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31 May 1973

General Support Maintenance Manual

TEST SET, SIGNAL DATA CONVERTER AN/AYM-8

(FSN 6625-137-2289)

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CHAPTER 1

INTRODUCTION

1-1. Scope

a. This manual provides general support maintenance instructions for Test Set, Signal Data Converter AN/AYM-8 (fig. 1-1). It includes an introduction, a description of the functioning of the equipment, general support maintenance instructions, and diagrams. The maintenance instructions cover troubleshooting, removal and replacement instructions, adjustment and alignment procedures, repair instructions, and testing procedures.

b. **Operator and organizational** maintenance **instructions are contained in TM** 11-6625-2479-**12.**

1-2. Indexes of Publications

a. DA Pam 310-4. **Refer to the latest issue of DA Pam 310-4 to determine whether there are new editions, changes, or additional publications pertaining to the equipment.**

b. ***DA*** **Pam** ***310-7.*** **Refer to the latest issue of DA Pam 310-7 to determine whether there are modification work orders (MWO's) pertaining to the equipment.**

NOTE

Applicable forms and records are covered in TM 11-6625-2479-12.

1-3. Reporting of Equipment Publication Improvements

The reporting of errors, omissions, and recommendations for improving this publication by the individual user is encouraged. Reports should be submittted on DA Form 2028 (Recommended Changes to Publications) and forwarded direct to Commander, US Army Electronics Command, ATTN: AMSEL-MA-SS, Fort Monmouth, NJ. 67703.

CHAPTER 2

FUNCTIONING OF EQUIPMENT

Section I. BLOCK DIAGRAM ANALYSIS

2-1. General

The block diagram analysis of the test set is given in two levels of discussion in this section. In the first level, the relationship between the test set and the Signal Data Converter CV-2647/AYA-10 (SDC) is explained (para 2-2). In the second level of discussion, each functional block within the test set is discussed separately (para 2-3).

2-2. Overall Block Diagram (fig. FO-2)

a. The test set is used to test the performance of the SDC. It does this by simulating the inputs and stimuli the SDC normally receives from other airborne avionics systems. The outputs of the SDC resulting from these inputs and the stimuli are monitored and displayed on the test set. This enables an operator to evaluate the performance of the SDC.

b. The test set is divided into the functional circuits shown as blocks. These circuits produce signals that the SDC normally receives from interfacing airborne systems. The data ready signal from the teat set informs the SDC that upgraded data is on its way. A data demand signal from the test set requests a data block for a specific camera or sensor. The SDC processes the simulated data inputs, a group at a time, and then generates display outputs. The display outputs are horizontal and vertical deflection signals and unblanking signals used to drive the DISPLAY CRT in the display select controls section of the test set. The display signals from the SDC arrive in a predetermined sequence. This sequence results in either a pattern of coded dots (excess three BCD) or in a number (numeric) on the DISPLAY CRT in the display select controls section of the test set.

c. The data demand controls produce any one of five output signals in response to manipulation of the DATA DEMAND controls of the test set. These outputs simulate the data demand signals from either the KA60-1, KA60-2, KA76, SLAR, or IR systems. When the SDC receives any of the five data demand signals, it responds by generating a three-level parallel binary data request word coded for the data demand line activated.

d. The data request word is formed by the signals present on the AL-l, AL-2, and AL-3 lines. When these signals arrive at the input of the data ready circuit in the test set, the data ready circuit responds by producing a data ready output to the SDC. This in turn causes the SDC to clear its registers and activate a sequence of unique data selection gates. These gates activate simulator circuits in the test set.

e. The test set supplies the SDC with fixed and variable data outputs. Some of these data are transmitted to the SDC upon receipt of specific negative pulses (the unique data selection gates) from the SDC. Other data outputs are continually produced at the test set.

f. The focal length data simulators respond to two of the unique data selection gates from the SDC. The response is in the form of outputs in excess-three BCD. These outputs simulate the data representing the focal length of the lens employed by the KA76 camera.

g. In a similar manner, the date, taking unit, and sortie data simulators respond to the unique data selection gates by producing a set of decimal-coded signals. These signals simulate the data representing the date (day, month, and year), the taking unit (squadron or aircraft), and the number of the sortie.

h. The time of day simulators respond to the TIA output signal of the SDC. This response is in the form of a two level, excess-three BCD data output word simulating the time of day (hours, minutes, and seconds). The data output of the

time of day simulators can also be entered into the SDC at any time by having the operator depress the TIME SET switch of the test set.

i. The barometric altitude sensor simulator receives a reference voltage (6.2 Vdc) from the SDC. The test set then sends back to the SDC a selectable portion of the 6.2 Vdc reference to stimulate barometric altitudes from zero to 10,000 ft. This information is continually updated without a request (no unique data selection gate required).

j. The remaining data simulators also produce their data outputs continually without a request. This group includes the exposure data simulator. the KA76 camera angular position, the IR filter simulators, the SLAR signal simulators, and the pitch and roll sensor simulators. These data simulators produce their outputs as a result of manipulation of front panel switches on the test set.

k. The exposure data simulator produces a BCD number on three lines. The BCD number simulates the exposure period of the KA66-1, KA60-2, or the KA76 camera.

l. The camera angular position and IR filter simulators produce discrete output signal levels corresponding to one of five possible conditions. Angular position is taken out on five separate lines. Only one of the five lines is activated at any time as a function of the setting of the KA-76 ANGULAR POSITION switch. The five positions simulate camera angular depressions of 15° right, 30° right, 0°, 30° left, and 15° left from the roll axis. The IR Alter data simulator produces an activating signal on one of five lines as a function of the IR FILTER switch position. The activated line corresponds to a data input to the SDC. The data input represents the selection of a particular filter by the IR system.

m. The SLAR signal simulators produce discrete output signals which simulate the SLAR range and range delay outputs to the SDC. SLAR range delay is an active signal level on one of seven lines, corresponding to delays of zero, 10, 20, 30, 40, 50, or 60 kilometers. The SLAR range signal is an active level on one of three lines, corresponding to ranges of 25, 50, or 99 kilometers.

n. Navigation data simulating northings eastings, heading, etc.) is produced as an up to 24-bit parallel word in excess-three BCD by the navigation data simulators.

o. Signals simulating the three-wire synchro outputs of the pitch and roll sensors are provided by precision pitch and roll ratio transformers in the test set. The operator of the test set can select any one of 13 roll or pitch simulation signals by manipulation of the PITCH and ROLL switches on the front panel of the test set.

p. To this point, we have discussed the generation of the data ready signal to the SDC and the production of the signals which simulate those from the airborne equipment the SDC normally interfaces. What happens now is that the SDC begins to produce the outputs which allow these data to be displayed on a CRT. The display can be a coded dot pattern (excess-three BCD) or a numeric display. The desired display can be selected at the test set by means of the MODE SEL switch (the mode control circuit). This switch allows the operator to choose any of three display modes: BCD, numeric, or alternating BCD and numeric.

q. The circuits which select the display drive outputs of the SDC and process them for display on the DISPLAY CRT are the display select controls. These allow the operator of the test set to select KA60 or KA76 data, SLAR data, IR data, or that which would be displayed on the CDM unit of Airborne Data Annotation System AN/AYA-10 (the ADAS). The display select circuitry also enables display. of the data on an external oscilloscope.

r. The remaining functional block IS that of system go no-go test, frame reset, and mode control. The mode control circuit generates the BCD, alternate, and numeric control signals. These signals determine the display mode in which the SDC is to operate. The system lamp test circuit generates the TEST signal to the SDC. This signal initiates a system go no-go test within the SDC. The GO NO-GO signal from the SDC indicates to the test set by a lamp lighting or not lighting whether or not the test is go or no-go. The frame reset circuit generates a signal which resets the photographic frame counter in the SDC and also checks the SYSTEM/NO-GO lamp.

2-3. Detailed Block Diagrams

The following paragraphs contain discussions of each of the test set circuit blocks shown in figure FO-2. In each case, the discussion is supported by a detailed block diagram or a simplified schematic of the circuit.

a. Data Demand Controls (fig. FO-3). The function of the data demand controls is to produce data demand signals simulating those which the SDC normally receives from the KA60-1 KA60-2, or KA76 cameras, the SLAR, or the IR equipment. The overall circuit is made up of the DATA DEMAND PULSE and PRIORITY switches on the front panel assembly 1A3, and logic components which are part of display and data demand-board 1A3A2. The circuit functions as follows: The operator decides which data he wishes to demand from the SDC and whether he wishes the data to be displayed on the DISPLAY CRT continuously or only once. He then sets KA-60 DATA DEMAND switch 1A3S5, SLAR DATA DEMAND switch 1A3S3, IR DATA DEMAND switch 1A3S2, or KA-76 DATA DEMAND switch 1A3S4 to SINGLE PULSE or CONTINUOUS DISPLAY, as desired. If KA60 data is chosen, the operator must also decide whether he wishes to demand data for the KA60-1 or KA60-2 camera by selecting the appropriate position of PRIORITY switch 1A3S7. If CONTINUOUS DISPLAY is chosen, the data demand controls start producing data demand signals on the lines for the system selected in a steady pulse train. If SINGLE PULSE is selected the data demand controls produce a single data demand and signal on the proper output line each time PULSE-switch 1A3S6 is depressed.

b. Data Ready Circuit (fig. 2-1 and 2-2). The function of the data ready circuit is to produce a data ready signal in response to active inputs on the AL-1, AL-2, and AL-3 (address line) signals from the SDC. The AL-1, AL-2 and AL-3 address lines carry parallel, three-level binary- coded- number representing a data demand from an avionics unit. The address number (AL-1 in the LSB) is incremented by one during each data ready cycle (18.2 MS). Thus, the progression is 000, 001, 010. 011, 100, 101, 110,

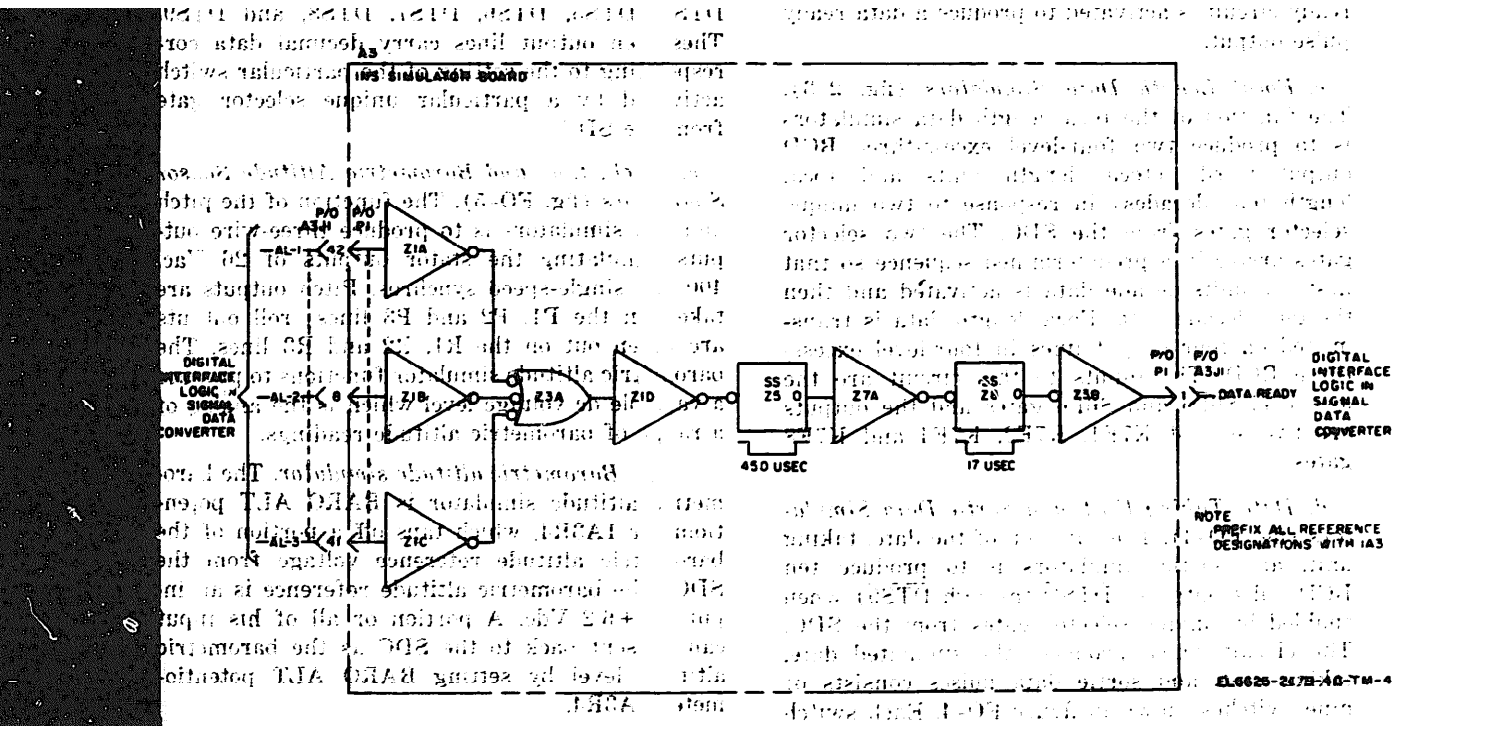


Figure 2-1. Data ready circuit, logic diagram.

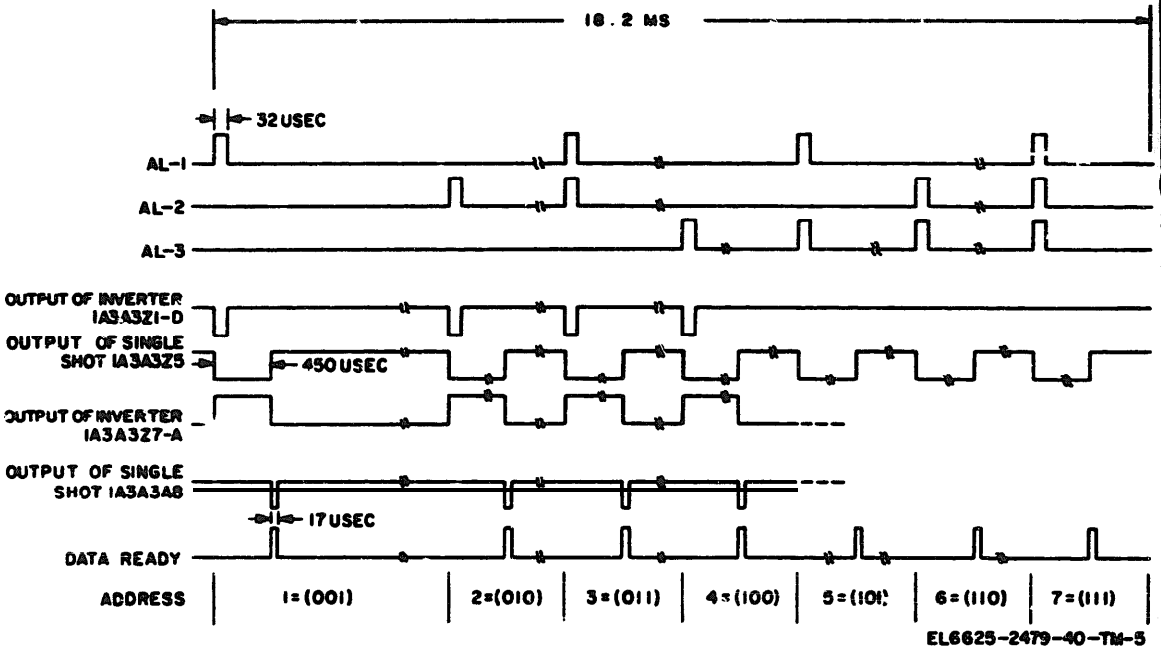


Figure 2-2. Data ready circuit, timing diagram.

111 and back to 000, and so on. So long as any of the three address line inputs go to a logic 1, or high level state during a data ready cycle, the data ready circuit is activated to produce a data ready pulse output.

c. Focal Length Data Simulators (fig. 2-3). The function of the focal length data simulators is to produce two four-level excess-three BCD output words (focal length units and focal length tens decades) in response to two unique selector gates from the SDC The two selector gates arrive in a predetermined sequence so that first the units decade data is activated and then the tens decade data. Focal length data is transmitted on four output lines in four-level excess-three BCD. The inputs to this circuit are the low level S6L5 and S6L6 gates and the outputs are two sets of K7F1, K7F2, K7F4 and K7F8 gates.

d. Date, Taking Unit, and Sortie Data Simulators (fig. FO-4). The function of the date, taking unit, and sortie simulators is to produce ten BCD pulse outputs (DTSO through DTS9) when enabled by unique selector gates from the SDC. The circuit which produces the simulated date, taking unit, and sortie data pulses consists of nine switches shown in figure FO-4. Each switch is enabled by one or more of the unique selector gates from the SDC. Note that all ten outputs of all the switches use common lines time-shared for the outputs: DTS0, $\overline{\text{DTS1}}$, DTS2. DTS3 DTS4, DTS5, $\overline{\text{DTS6}}$, DTS7, DTS8, and DTS9 These ten output lines carry decimal data corresponding to the setting of the particular switch activated by a particular unique selector gate from the SDC.

e. Pitch, Roll, and Barometric Altitude Sensor Simulators (fig. FO-5). The function of the pi and roll simulators is to produce three-wire outputs simulating the stator outputs of 26 Vac 400 Hz, single-speed synchros. Pitch outputs are taken on the P1, P2 and P3 lines; roll outputs are taken out on the R1, R2 and R3 lines. The barometric altitude simulator functions to produce a variable dc voltage level which is the analog of a range of barometric altitude readings.

(1) Barometric altitude simulator. The barometric altitude simulator is BAR0 ALT potentiometer 1A3R4, which taps off a portion of the barometric altitude reference voltage from the SDC. The barometric altitude reference is an input of +6.2 Vdc. A portion or all of his input can be sent back to the SDC as the barometric altitude level by setting BAR0 ALT potentiometer 1A3R4.

(2) Roll simulator. The roll simulator cir-

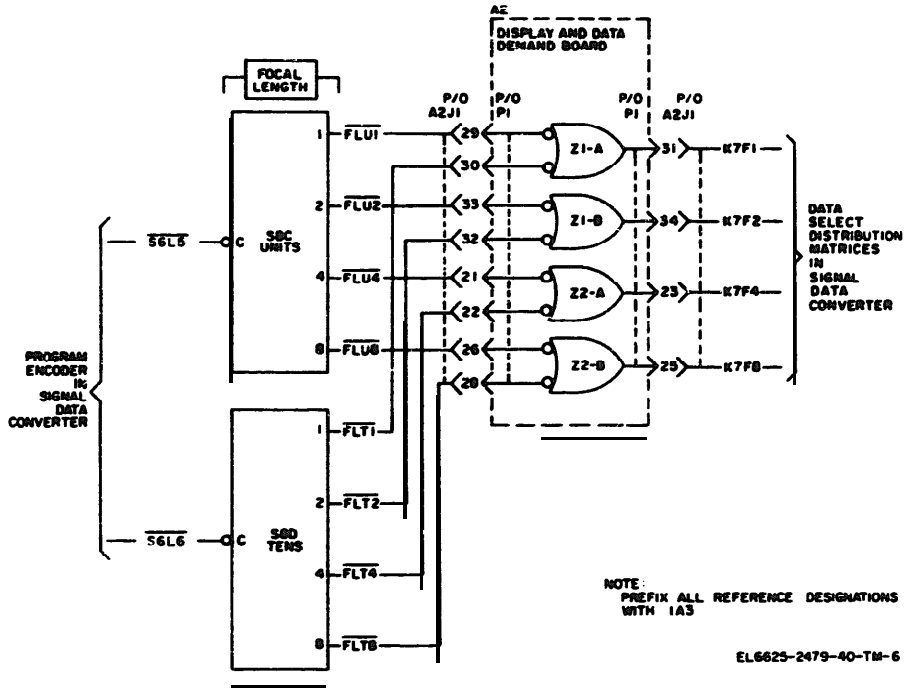


Figure 2-3. Focal length data simulators, block diagram.

cuit is made up of roll ratio transformer 1A3A5-T1 and ROLL switch 1A3A5S1. A continuous 26 Vac, 400 Hz input from power supply 1A3A1 is applied across the primary of ratio transformer 1A3A5T1. The secondary of the ratio transformer has 14 voltages available at its output (VR1. through VR14). These output voltages are connected to ROLL switch decks lA3A5S1-A, -B, and -C as shown in figure FO-5. When **ROLL switch 1A3A5S1 is set to a particular roll position, one of each of the voltages on each of three decks is transferred to the output side as R3, R2, and R1. Between any pair of these three output wires, the maximum voltage does not exceed 11.8 Vac. Each combination of voltage levels corresponds to one of 13 possible simulated roll** &placement readings to the SDC.

(3) Pitch simulator. The pitch simulator circuit is made up of pitch ratio transformer 1A3A5T2 and PITCH switch 1ASA5S4. The operation of this circuit is identical to that of the roll simulator as described in (2) above.

f. Time of Day Simulators (fig. 2-4). The function of the time of day simulators is to produce two sets of outputs (units and tens) in excess-three BCD in response to either a TIA clocking gate from the SDC or to the activation of TIME SET switch l13S11 on the test set.

g. Exposure Data Simulator (fig. 2-5). The function of the exposure data simulator is to produce a parallel three-bit number used by the SDC to select camera exposure periods for the KA60-1, KA60-2, and KA76 cameras. The circuit consists of EXPOSURE switch 1A3S10-A, on which the operator of the test set can select

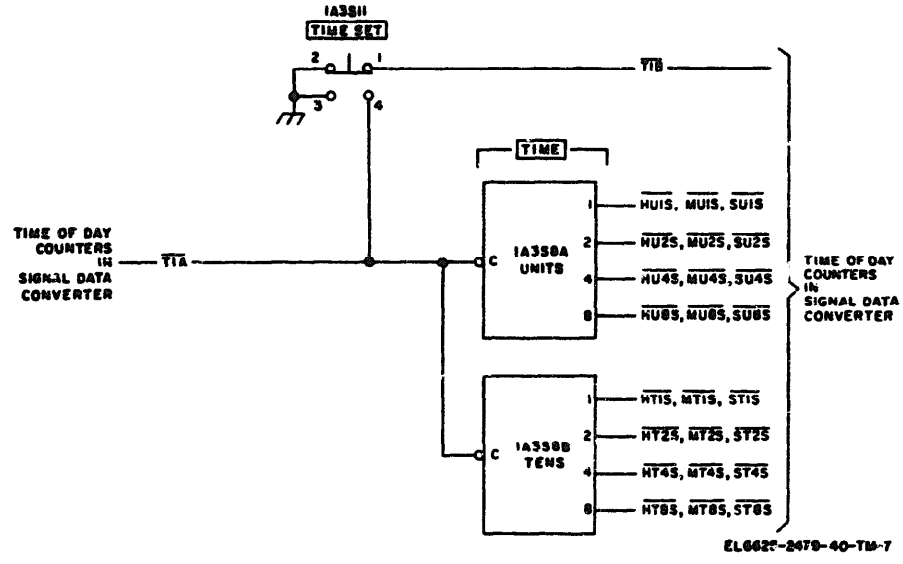


Figure 2-4. Time of day simulators, block diagram.

any of 8 decimal numbers (0 through 7). EXPOSURE switch 1A3S10-A has its common (C) side tied to ground, enabling it to transfer ground to three output lines EXP1, EXP2, and EXP4 (ground is active level).

h. Camera Angular Position and IR Filter Simulator (fig. Z-6). The camera angular position simulator consists of KA-76 ANGULAR POSITION switch 1A3A5S5 and a +28 Vdc pull-up network. Switch 1A8A5S5 has five positions which correspond to angular depressions from the aircraft roll axis of 15°L, 30°L, 0°, 30°R, and **15°R, respectively. The** switch transfers ground **to the signal line to be** activated. Position 3 of **switch 1A3A5S5 is not** connected on the output **side. Hence, when the** switch is in this position **(corresponds to 0° di**splacement), + 28 Vdc is **placed** on all four of the output lines, The IR Alter simulator consists of IR FILTER switch

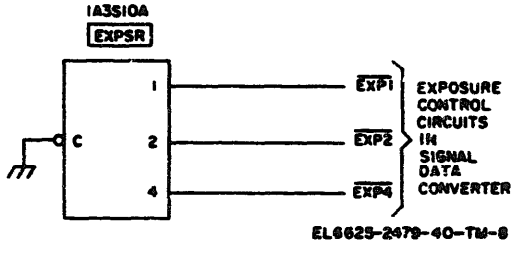


Figure 2-5. Exposure data simulators, block diagram.

1A3A5S6, decks A and B. The switch places ground on any one of the five output lines selected to the SDC, and +28 Vdc on the remaining four. The ground signal determines which IR filter is to be simulated.

i. STAR Signal Simulators (fig. 2-7). The function of the SLAR signal simulators is to provide SLAB range delay and SLAR range signals to the SDC. These signals are produced in response to the setting of SLAR RANGE DELAY switch 1A3A5S2 and SLAR RANGE switch 1A3A5S8.

(1) SLAR RANGE DELAY switch 1A3A5S2 transfers +28 Vdc to any one of seven output lines (SLRO through SLR6). The output line so activated, represents a particular SLAB range delay to the SDC. The seven range delays are 0, 10, 20, 30, 40, 50, or 60 kilometers.

(2) SLAR RANGE switch 1A3A5S3 transfers + 28 Vdc to one of three output Sines : 1RW1, 1RW2, or 1RW3. The line so activated simulates one of the three possible SLAR operating ranges to the SDC. The three ranges simulated **are 25 Km** (1RW1), 50 Km (1RW2) or 99 Km **(1RW3).**

j. Navigation Data Simulators **(fig. FO–6).** The function of the navi**gation data simulators** is to continually produce navigation data words consisting of up to 24 data bits to the SDC. A data word is sent in six decade levels (10°, 10^1 through 10°), four bits per decade, in excess-

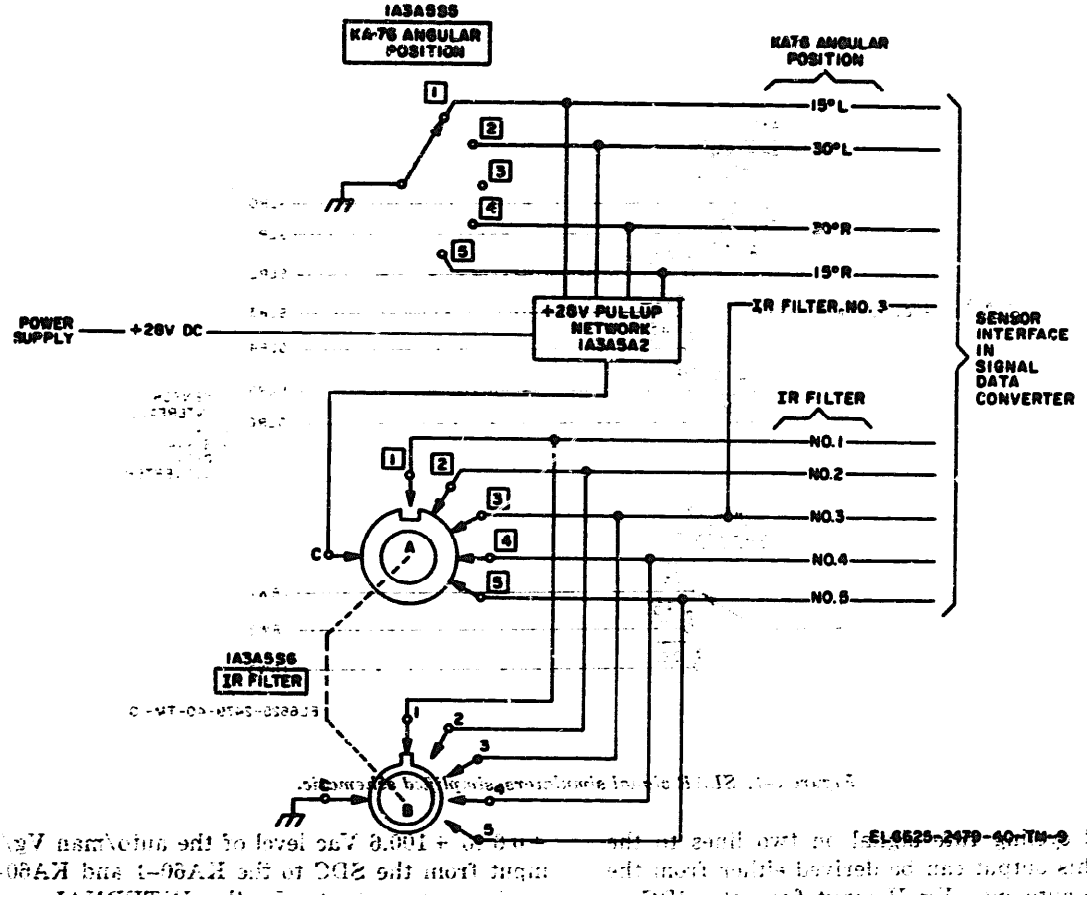


Figure 2-6. Camera regular position and IR filter simulators, simplified schematic.

three BCD. The content of the word (the number it represents) simulates navigation digital data, such as northings, eastings, and heading, that the SDC normally receives from airborne navigation equipment.

k. Display Select Controls (fig. FO–7). The function of the display select controls is to allow the test set operator to choose the data he wishes presented on the DISPLAY CRT. The display select controls also has circuitry that enables the operator to present the identical data present on the DISPLAY CRT on an external oscilloscope simultaneously.

(1) The display select controls circuit is made up of DISPLAY SELECT switch 1A3A5S7; electrostatic DISPLAY CRT 1A3A5A4V1 and its associated controls, biasing, unblanking and intensity control networks; a SCOPE Y terminal for external vertical deflection outputs; a SCOPE X terminal, impedance matching network and attenuator network for external horizontal deflection outputs; and a SCOPE Z connector with unblanking control network and signal pulse driver (amplifier) for external unblanking signal outputs.

(2) In general, the display select controls circuit operates as follows: The operator chooses any one of six functional groups of data from the SDC he wishes to display. Then, by setting DISPLAY SELECT switch 1A3A5S7 at the position corresponding to the data group chosen, DISPLAY CRT 1A3A5A4V1 receives the proper horizontal drive, vertical drive, and unblanking signals from the SDC. Aside from power inputs, five separate signals are required to form a display on CRT 1A3A5A4V1; horizontal deflection (−), horizontal deflection (+), vertical deflection (+), vertical deflection (−), and unblanking signals.

l. Cycling Rate Controls (fig. 2–8). The function of the cycling rate controls is to produce a variable dc voltage simulating the KA60–1 and

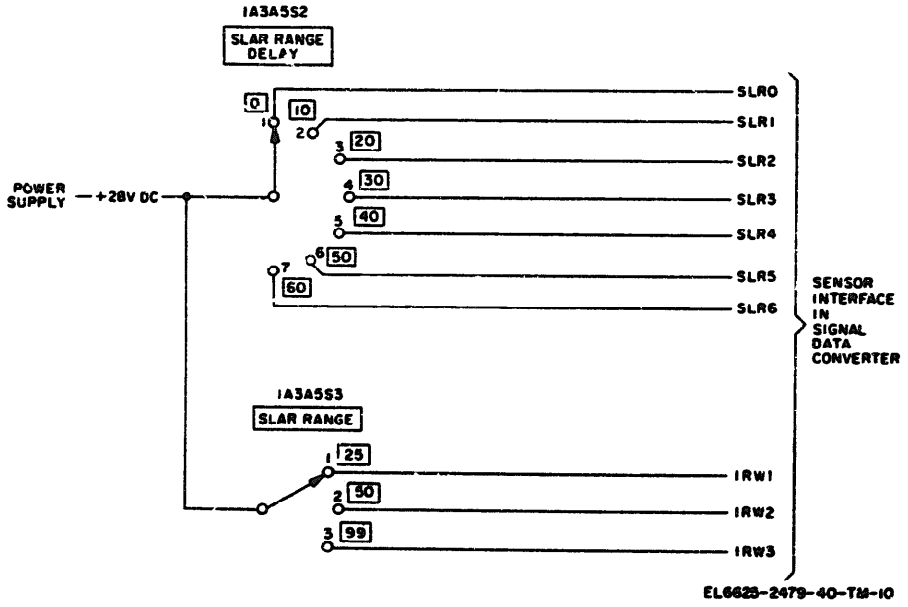


Figure 2-7. SLAR signal simulators, simplified schematic.

KA60-2 cycling rate signal on two lines to the WC. This output can be derived either from the variable auto/man Vg/H input from the SDC or from' a variable dc source within the test set. The circuit which permits selection of the source of the cycling rate signal and which varies the level generated from the test set is shown in fig. 2-8. This consists of CYCLING RATE switch 1A3S1 and potentiometer 1A3R3. In the EXTERNAL position, switch 1A351 transfers the +0.6 to +100.6 Vac level of the auto/man Vg/H input from the SDC to the KA60-1 and KA60-2 cycling rate outputs. In the INTERNAL position, switch 1A3S1 transfers that portion of a + 100 Vdc level from power supply 1A3A1 which is tapped off by potentiometer 1A3R3.

m. System Lump Test, Frame Reset, and Mode Control (fig. 2-9). This group of controls functions to generate the system lamp test signals, the signal which resets the frame counter for

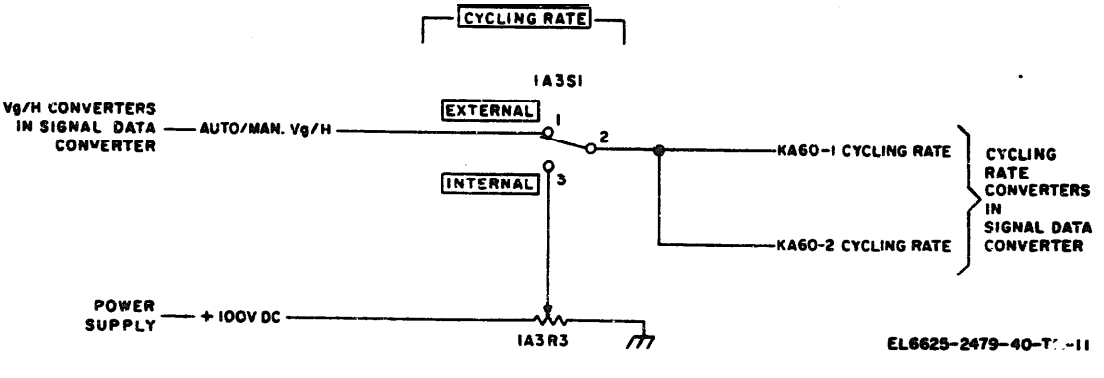


Figure 2-8. Cycling rate controls, simplified schematic.

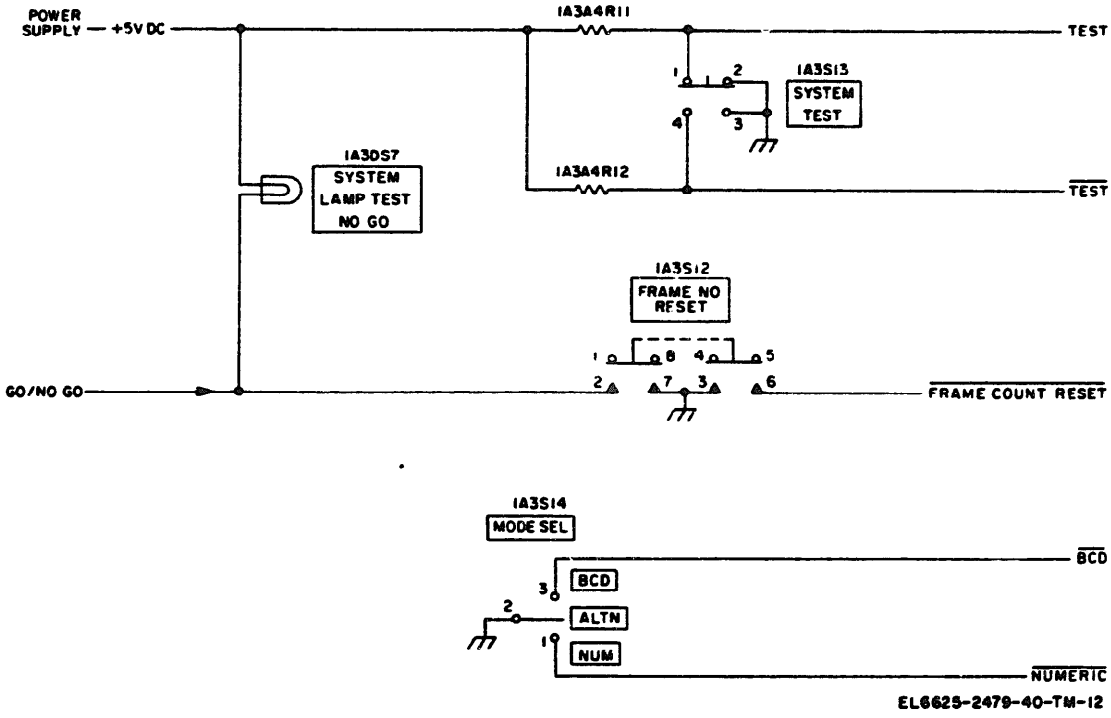


Figure 2-9. System tamp teat, frame reset, and mode control, simplified schematic.

he camera and sensor system, and the control signals which direct the SDC to produce its display outputs in either BCD, numeric, or alternating BCD and numeric form. Further, this circuit also responds by lighting an indicator lamp if the signal generated by the test circuitry in the SDC indicates a no-go condition in the SDC.

n. Power Supply (fig. FO-8). The power sup ply distributes or produces the ac and dc power required for the SDC and the test set. It receives +28 Vdc and 115 Vac, 400 Hz, inputs from external power sources and produces Altered +28 Vdc, filtered 115 Vac, 400 Hz, and distributes unfiltered 115 Vac, 400 Hz and +28 Vdc to the SDC. It also produces regulated +5 Vdc for the battery simulator in the SDC, the logic circuits and +5 Vdc lamp in the test set. The power supply also produces 26 Vac, 400 Hz and regulated 100 Vdc for the SDC.

Section II. DETAILED CIRCUIT ANALYSIS

2-4. General

This section provides **detailed circuit descriptions** of the functional **circuit groups described** in chapter 2, section I **of this manual. The purpose** of this section is to describe those details of the circuit not given at the block diagram level.

NOTE

In the following circuit discussions, **certain logic conventions are assumed.** They **are—**

1. A logic low level means ground, or zero + 001 dc.
2. A logic high level means open, or +5 ±0.5 Vdc.

2-5. Data Demand Controls (fig. FO-9 and FO-3)

***a.* The +5 Vdc return line from the power** supply is tied to the input side of all four DATA DEMAND switches 1A3S2, S3, S4, and S5 as well as PULSE switch 1A3S6. The switches transfer the +5 Vdc return as a logic low level to

activate the circuits on display and data demand board 1A3A2. The outputs of these circuits are the KA60, KA76, IR or SLAB data demand pulses.

b. With KA-60 DATA DEMAND switch 1A3S5 at OFF, an open, or high level input is presented to interface buffers 1A3A2Z5C and 1A3A2Z5D. This causes them to produce low level outputs (their inactive states). These low level outputs inhibit AND gates 1A3A2Z9A and 1A3A2Z9B, thereby preventing any signals from passing through them out to the KA60 output lines.

c. When KA-60 DATA DEMAND switch 1A3S5 is set to CONTINUOUS DISPLAY, a logic low level (ground) is transferred through it to activate interface buffer 1ASA2Z5C. Interface buffer 1A3A2Z5C, when so activated, produces a logic high level output to condition AND gate 1A3A2Z9B. With this conditioning, AND gate 1A3A2Z9B will produce a low level output each time the input from divide-by-two flip-flop 1A3A2Z7 goes to high level.

d. Flip-flop 1A3A2Z7 is triggered by a free running generator which produces a symmetrical pulse train output with a prf of 23 Hz (fig 2-10). This output is applied to the clock pulse input of divide-by-two flip-flop 1A3A2Z7. Each time the pulse train signal makes a transition from high level to low level, flip-flop 1A3A2Z7 changes output states. Hence, at its 1 output it produces a square wave pulse train with a prf of 14 Hz.

e. The output of divide-by-two flip-flop 1A3A2Z7, along with the high level conditioning signal from interface buffer 1A3A2Z5C, activate AND gate 1A3A2Z9B to produce a low level output each time the two inputs are at coincident high levels. Single shot 1A3A2Z11 fires each time the output of AND gate 1A3A2Z9B makes a transition from high level to low level. When it fires, single shot 1A3A2Z11 produces a 600-microsecond-wide low level pulse at its 0 output. These low level pulses activate inverter 1A3ABZ6D to produce high level outputs which are amplified by line drivers 1A3Z1A and 1A3Z1B. The high level pulses are then routed to either the KA60-1 data demand output line or the KA60-2 data de-

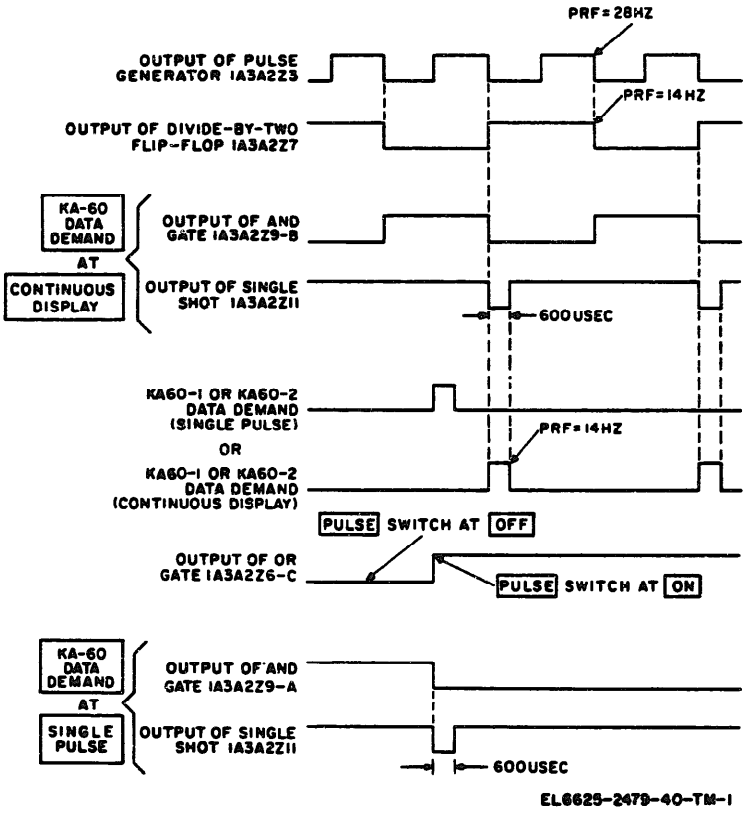


Figure 2-10. KA60 data demand controls, timing diagram.

mand output line, through PRIORITY switch 1A3S7.

f. When KA-60 DATA DEMAND switch 1A-3S5 is set to SINGLE PULSE, the low level transferred through it activates interface buffer 1A3A2Z5D to produce a high level output. This high level output is used to condition AND gate 1A3A2Z9A. AND gate 1A3A2Z9A can not be activated by a high level input from single pulse enable flip-flop 1A3A2Z6B and C.

g. The single pulse enable flip-flop produces a high level signal at its 1 output each time PULSE switch 1A3S6 is depressed, as follows: With PULSE switch 1A3S6 released. a low level is transferred through it to reset flip-flop 1A3-A2Z6B and C. In the reset state the 1 output of flip-flop 1A3A2ZGB and C is at low level, inhibiting AND gates 1A3A2Z9A, Z8B, Z8C, and Z9D. When PULSE switch 1A3S6 is depressed, the low level transferred through it sets flip-flop 1A3A2Z6B and C to produce a high level at its 1 output. This output remains at high level (active state) as long as the PULSE switch remains in the depressed position. It returns to low level when the PULSE switch is released.

h. When flip-flop 1A3A2Z6B and C is set, AND gate 1A3A2Z9A is activated to produce a low level output pulse. Single shot 1A3A2Z11 fires as the output of AND gate 1A3A2Z9A makes its high level to low level transition, producing a single 600 microsecond-wide low level pulse at its 0 output. As with the train of pulses generated in the continuous display mode (e above), the low level pulse activates inverter 1A3A2Z6D and line drivers 1A3Z1A and 1A3-Z1B to produce a high level pulse on the KA60-1 DATA DEMAND or KA60-2 data demand output lines through PRIORITY switch 1A3S7.

i. **With KA–76 DATA DEMAND switch 1A-3S4 at OFF, an open line input is presented to interface buffers 1ASA2Z5B and 1A3A2Z5A. This causes them to produce low level outputs (their inactive states). These low level outputs inhibit AND gates 1A3A2Z9C and 1A3A2Z9D, thereby preventing any signals from passing through them and out to the KA76 output lines.**

j. **When KA–76 DATA DEMAND switch 1A-3S4 is set to CONTINUOUS DISPLAY, a logic low level is transferred through it to activate interface buffer 1A3A2Z5B. When so activated, interface buffer 1A3A2Z5B produces a logic high level output to condition AND gate 1A3A2Z9C. With** this conditioning@ AND **gate 1A3A2Z9C** -produces a low level output **each time the input** from divide-by-two flipflop **1A3A2Z7 goes to** high level (d above). E**ach time the output of** AND gate 1A3A2Z9C makes the transition from high to low level, single shot 1A3A2Z10 fires.

k. When it Ares, single shot 1A3A2Z10 produces a 20 millisecond-wide low level pulse at its 0 output. The low level output pulses are applied to the base of transistor switch 1A3A2Q3 to bias it off.

l. Transistor switch 1A3A2Q3 inverts and amplifies the output of single shot 1A3A2Z10. In **its** quiescent state,. single shot 1A3A2Z10 produces **a steady logic high level** output which keeps transistor **switch 1A3A2Q3** conducting. In this state, **the collector is at low** level. This low is felt on **the KA76 data demand line.**

***m.* When single shot 1A3A2Z10 fires, the logic low level output pulse cuts off transistor switch 1A3A2Q3 for the duration of the pulse, allowing the +28 Vdc on its collector to be felt on the KA76 data demand output line to the SDC. Figure 2–11 shows the timing of these pulses.**

***n.* When KA–76 DATA DEMAND switch 1A-3S4 is set to SINGLE PULSE, the low level transferred through it activates interface buffer 1A3A2Z5A to produce a high level output. This high level output is used to condition AND gate 1A3A2Z9D. AND gate 1A3A2Z9D can now be activated by a high level from single pulse enable flip-flop 1A3A2Z6B and C. Refer to *g* above for an explanation of how the single pulse enable flip-flop is activated by PULSE switch 1A3S6.**

***o.* When the 1 output of flip-flop 1A3A2Z6B and C makes the transition from low level to high level, AND gate 1A3A2Z9D is enabled to produce a low level pulse to fire single shot 1A-3A2Z10. Refer to *k, l,* and *m* above for explanation of how the KA76 data demand pulse is generated from the output of single shot 1A3A2Z10.**

***p.* With SLAR DATA DEMAND switch 1A-3S3 at OFF, logic high level inputs are presented to interface buffers 1A3A2Z5E and 1A3A2Z5F. This causes them to produce low level outputs which inhibit AND gates 1A3A2Z8A and 1A3-A2Z8B, thereby preventing any signals from passing through them and out to the SLAR output lines. (Refer to fig. 2–12.)**

***q.* When SLAR DATA DEMAND switch 1A-3S3 is set to CONTINUOUS DISPLAY, a logic low level is transferred through it to activate interface buffer 1A3A2Z5F. Interface buffer 1A-**

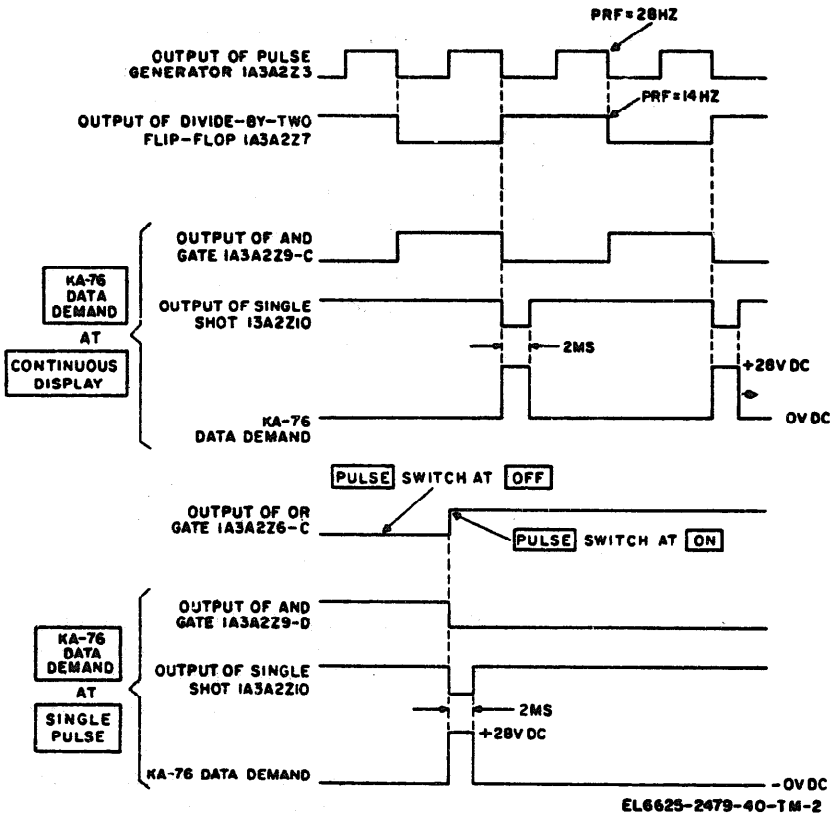


Figure 2-11. KA76 data demand controls, timing diagram.

3A2Z5F then produces a high level output to condition **AND gate 1A3A2Z8A.** With this conditioning, **AND gate 1A3A2Z8A** produces a low **level output** each time the input from divide-by-**two flip-flop 1A3A2Z7 goes to high level (*d* above). The output of AND gate 1A3A2Z8A is applied to the base** of transistor switch 1A3A2Q2 **through a wired OR connection.**

***r.* When SLAR DATA DEMAND switch 1A-3S3 is set to SINGLE PULSE, a logic low level is transferred through it to activate interface buffer 1A3A2Z5E. Interface buffer 1A3A2Z5E then produces a high level output to condition AND gate 1A3A2Z8B. With this conditioning, AND gate 1A3A2Z8B produces a low level output each time the output of flip-flop 1A3A2Z6B and C goes to high level (*g* above). The output of AND gate 1A3A2Z8B is applied to the base of transistor switch 1A3A2Q2 through a wired OR connection.**

***s.* In its quiescent state (SLAR DATA DEMAND switch 1A3S3 at OFF) transistor switch 1A3A2Q2 is conducting. This is so because both AND gates 1A3A2Z8A and 1A3A2Z8B are inhibited** and therefore apply +5 Vdc to the base of transistor switch 1A3A2Q2. With transistor switch 1A3A2Q2 conducting, a low level is on the SLAR data demand line to the SDC.

t. When either AND gate 1A3ABZ8A or 1A3-A2Z8R is activated to produce a low level output pulse, transistor switch 1ASA2Q2 is cut off. Transistor switch 1A**3A2Q2 remains** cut off for the period of time its **base receives the** logic low level. During that time, the +28 Vdc at its collector is placed on the SLAR data demand line.

u. The IR data demand signals **are** produced by the circuit made up of IR DATA DEMAND **switch 1A3S2, interface buffers 1A3A2Z4F and 1A3A2Z4D and gates 1A3A2Z8D and 1A3A2Z8C, and transistor switch 1A3A2Q1. The operation of this circuit is identical to that of the SLAR data demand controls (*p* above).**

2-6. Data Ready Circuit

(fig. FO-9 (2) 2-1, and 2-2).

This circuit is made up of logic com**ponents** which are part of INS simulator board **1A3A3.**

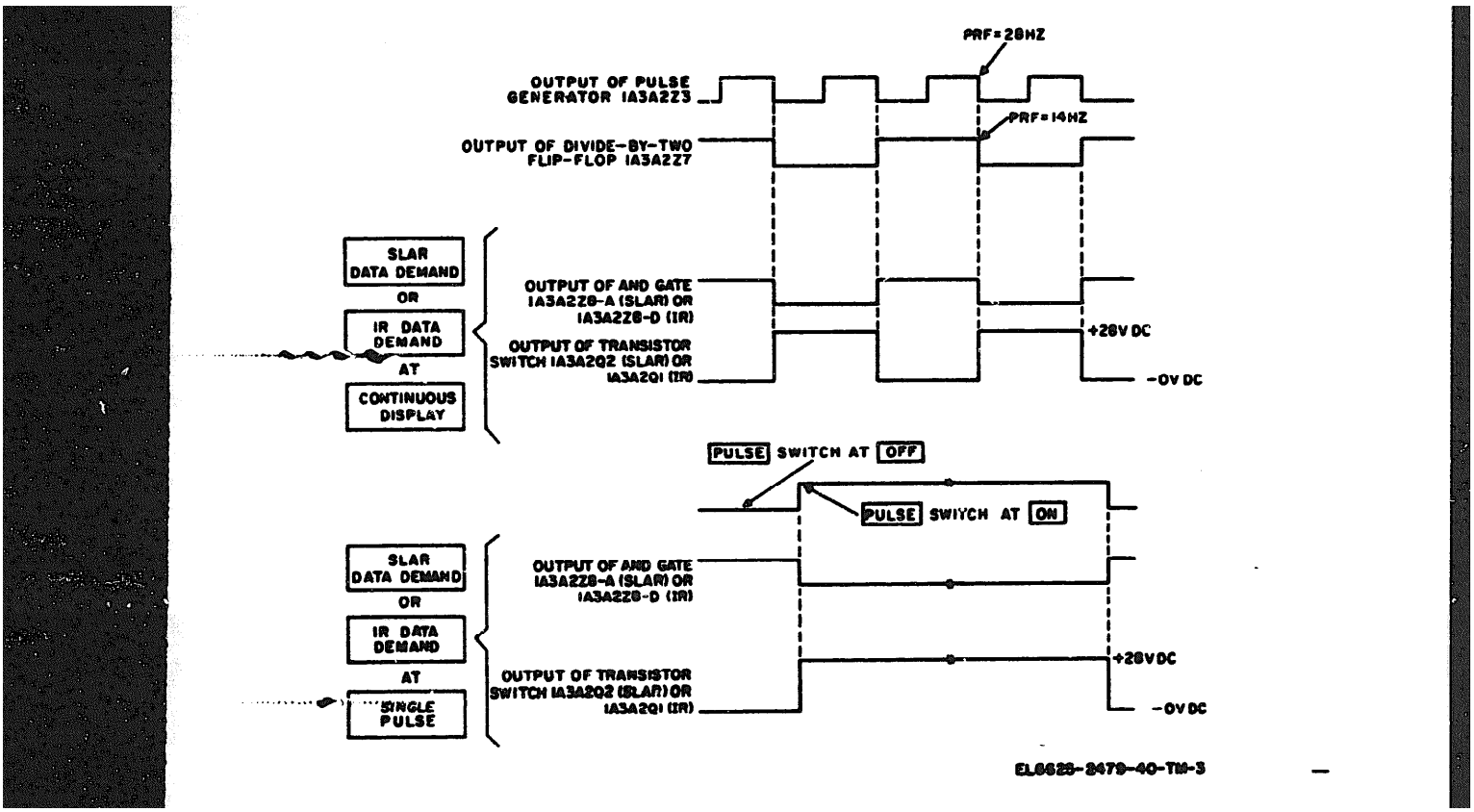


Figure 2-12. SLAR or IR data demand controls, timing diagram.

The inputs to the circuit are the AL–1, AL–2, and AL–3 address line signals from the SDC, and the output of the circuit in the data ready pulse.

a. The AL–1, AL–2, and AL–3 inputs are three-level BCD code words (7 words in a preset order) from the SDC, each representing a request for data. The three parallel inputs for each word arrive at the rate of seven addresses per 18.2 milliseconds. If any or all of the AL–1, AL–2, or AL–3 inputs make the transition from low to high level, the data ready circuit responds by producing a logic high level data ready pulse back to the SDC after a 450-microsecond delay period.

b. The AL–1, AL–2, and AL–3 inputs are 32 microsecond-wide pulses. These pulses arrive as shown in fig. 2–2 to form a set of specific address words. A high level on any of the three lines activates the inverter element associated with it (1A3A3Z1A for AL–1, 1A3A3Z1B for AL–2, and 1A3A3Z1C for AL–3). When any (or all) of these inverters are activated, they produce a low level pulse output to OR gate 1A3A3Z3A. This activates OR gate 1A3A3Z3A to produce a high level pulse output which is inverted to low level by inverter 1A3A3Z1D and sent to single-shot 1A3A3Z5.

c. Single-shot 1A3A3Z5 fires on the high-to-low level transition (leading edge) of the pulse from inverter 1A3A3Z1D, to produce a 450-microsecond low level pulse at its 0 output. The output of single-shot 1A3A3Z5 is inverted to high level by inverter 1A3A3Z7A and sent to trigger single-shot 1A3A3Z8.

d. Single-shot 1A3A3Z8 fires on the high-to-low level transition (trailing edge) of the pulse from inverter 1A3A3Z7A.

e. The 17 microsecond-wide low level pulse from the 0 output of single shot 1A3A3Z8 is inverted to high level by inverter 1A3A3Z3B and sent back to the SDC as the data ready pulse. The data ready pulse is generated 450 microseconds after each code word (set of AL–1, AL–2, and AL–3 pulses) is received.

2-7. Focal Length Data Simulators (fig. FO-9 and 2-6)

a. The focal length data simulators respond to

the S6L6 and S6L5 single inputs from the SDC by generating outputs on the K7F1, K7F2, K7F4, and K7F8 output lines to the SDC. The low level S6L6 and S6L5 inputs are applied to the common (C terminal) of FOCAL LENGTH TENS switch 1A3S8-D and UNITS switch 1A3S8-C through pins s and x, respectively, of CONTROL MONITOR connector 1A3J3.

b. Each deck of FOCAL LENGTH thumbwheel switches 1A3S8C and 1A3S8D responds to a low level input at its C termination by producing an excess-three BCD output on its four output lines (1, 2, 4, 8). An activated line produces a logic low level, an inactive line a logic high level.

Example: If the decimal number set on the FOCAL LENGTH units switch 1A3S8C were a 5, the excess-three BCD coding would be 1000, and the four output lines of switch deck 1A3S8C would be:

8	4	2	1
0 Vdc	5 Vdc	5 Vdc	5 Vdc

c. The outputs of each switch deck, enabled in turn, are applied to the OR gates, whose activated outputs are the high level simulated focal length signals K7F1, K7F2, K7F4, and K7F8. These signals are on the line only for as long as the switches are pulsed by the unique selector gates S6L5 and S6L6 from the SDC. Initially, both the S6L5 and S6L6 inputs are at high level (inactive). In this condition, all the outputs of both FOCAL LENGTH switch decks are at high - level (inactive). These high levels keep the outputs of all four OR gates (K7F1, K7F2, K7F4, K7FS) at low level (inactive).

d. The first signal input from the SDC is that of S6L5, a logic low level pulse, 192 microseconds wide. During the time that S6L5 is present, S6L6 remains inactive (at high level). The low level S6L5 enables FOCAL LENGTH units switch 1A3S8–C to release its data output to the four OR gates on data displaydemand board 1A3A2. Depending on the number set on the switch, one or more of these lines will have active (low level) outputs. Any line with a low level output activates its associated OR gate. For instance, taking the number used in the example preceding, the FLU(8) output line of switch 1A3S8-C is at low level and all others are high level. The FLU(8) activates OR gate 1A3A2Z2B to produce a high level output. OR gates 1A3A2Z1A, 1A3A2Z1B, and 1A3A2Z2A receive high level inputs and therefore produce low level (inactive) outputs. Thus, the decimal number 5 (1000 in excess three BCD) produces the following outputs on the focal length simulator output lines :

K7F8	K7F4	K7F2	K7F1
5 Vdc	0 Vdc	0 Vdc	0 Vdc

e. After the S6L5 input returns to high level, the S6L6 goes to low level for 192 microseconds. This enables FOCAL LENGTH tens decade switch 1A3S8-D to produce its data outputs. The operation of this sequence is the same as that just described.

2-8. Data Taking Unit, and Sortie Data Simulators

(fig. FO-9③)

a. Each of the nine thumbwheel switches making up DATE switch 1A3S10 (six thumbwheels) and those of SORTIE AND TAKING UNIT switch 1A3S8 (three thumbwheels) which are used in this circuit are enabled individually and in turn by gated input pulses from the SDC. These input signals, the switch the deck they enable, and the outputs enabled are listed in table 2-l.

b. The outputs of the switches are taken, in turn, as groups of DTS0 and DTS1 through DTS9 signals to the SDC. Resistors 1A3A4R1 through 1A3A4R10 maintain the voltage on these output lines to +5 Vdc during those intervals of time when there are no active (ground level) output signals from the DATE or SORTIE AND TAKING UNIT switches.

c. Note that some switch outputs are not used. Since the number of days in a month will not exceed 31, the 4-9 outputs of DATE-DAY switch 1A3S10-G (tens decade) are not needed. Similarly, the 2-9 outputs of DATE-MONTH switch 1A3S10-E (tens decade) are not needed since only 12 months are used.

d. The unique selector gate inputs (S5L2, S5L3, etc.) remain at logic low level to enable a switch for 192 microseconds. That means that the outputs of this circuit (DTS0-DTS9) are also low level pulses of 192 microsecond width. Since these are decimal bit signals, only one of the ten outputs is low at any time. Thus, if DATE-DAY switch were dialed to 21, indicating the 21st day of the month, only the DTS1 output of switch 1A3S10-F would be at low level when the S5L2 input was enabled. Then, only the DTS2 output of switch 1A3S10-G would be at low level when S5L3 was enabled.

Table 2-1. Date, Taking Unit, and Sortie Data simulator Functions

Unique selector gate input	*Switch activated*	*Decimal output on DTSO through DTS9 represents*
S5L2	DATE-DAY switch 1A3S10F	Units decade (0–9) of day of month (10^0).
S5L3	DATE-DAY switch 1A3S10G	Tens decade (0–3 only) of day of month (10^1).
S5L4	DATE-MONTH switch 1A3S10D	Units decade (0–9) of month of year (10^0).
S5L5	DATE-MONTH switch 1A3S10E	Tens decade (0 and 1 only) of month of year (10^1).
S5L6	DATE-YEAR switch 1A3S10B	Units decade (0–9) of year (10^0).
S5L7	DATE-YEAR switch 1A3S10C	Tens decade (0–9) of year (10^1).
S5L9, S5L16	SORTIE switch 1A3S8E	Units decade (0–9) of sortie (10^0).
S5L10, S6L1	SORTIE switch 1A3S8E	Tens decade (0–9) of sortie (10^1).
S5L11, S6L2[1]	SORTIE switch 1A3S8F	Hundreds decade (0–9) of sortie (10^2).
S5L12, S6L3[1]	SORTIE switch 1A3S8F	Thousands decade (0–9) sortie (10^3).
S5L13[2]	TAKING UNIT switch 1A3S8G	Units decade (0–9) of taking unit identification number (10^0).
S5L14[2]	TAKING UNIT switch 1A3S8G	Tens decade (0–9) of taking unit identification number (10^1).

[1] These numbers represent the hundreds and thousands decades of the combined sortie and taking unit.
[2] These numbers also represent the ten thousands and hundred thousands decades of the combined sortie and taking unit number.

2-9. Pitch, Roll, and Barometric Altitude Sensor Simulators

(fig. FO-9 ⑤)

a. Pitch Sensor Simulator. This circuit receives a 26 Vac, 400 Hz input from the power supply and produces ac outputs on three wires (P1, P2, and P3), the voltage ratios among the three-of which are made to vary as a function of the setting of PITCH switch 1A3A5S4.

(1) A 26 Vac, 400 Hz input from the power supply is applied across the primary of ratio transformer 1A3A5T2 through pins A and B of connector 1A3A5P4. The secondary of the ratio transformer taps off fourteen separate ac voltage levels which are applied to the three ganged decks of PITCH switch 1A3A5S4 as shown.

(2) PITCH switch 1A3A5S4 has 13 functional positions, each one corresponding to a particular pitch angle. When it is set to any of the 13 positions, each deck transfers the voltage applied to it in that position. This results in three separate voltages on three output lines. The output of switch 1A3A5S4–C is the P1 line; the output of 1A3A5S4–B is the P2 line; the output of 1A3A5S4–A is the P3 line. These three lines correspond to the stator output of a synchro. The ratio of the voltages on the three output lines for each functional position of PITCH switch 1A3A-5S4 is shown in table 2–2.

Table 2-2. PITCH Switch Positions and Corresponding Ratios

PITCH switch 1A3A5S4 position	*Ratio of voltages on outputs* $\left(\frac{P1-P3}{P1-P2}\right)$
+9	+0.168
+7	+0.132
+5	+0.096
+3	+0.059
+2	+0.040
+1	+0.020
0	0.000 (P1–P3) = (P1–P2)
−1	−0.020
−2	−0.040
−3	−0.059
−5	−0.096
−7	−0.132
−9	−0.168

b. Roll Sensor Simulator. This circuit receives a 26 Vac, 400 Hz input from the power supply and produces ac outputs on three wires (R1, R2 and R3), the voltage ratios of which are made to vary as a function of the setting of ROLL switch 1A3A5S1.

(1) A 26 Vac, 400 Hz input from the power supply is applied across the primary of ratio transformer 1A3A5T1 through pins A and B of connector 1A3A5P4. The secondary of the ratio transformer taps off fourteen separate ac voltage levels which are applied to the three ganged decks of ROLL switch 1A3A5S1 as shown.

(2) ROLL switch 1A3A5S1 has 13 functional positions, each one corresponding to a particular roll angle. When it is set to any of the 13 positions, each deck transfers the voltage applied to it in that position. This results in three separate voltages on the three output lines. The output of switch 1ASA5S1-C is the R1 line; the output of switch 1A3A5S1-B is the R2 line; the output of switch lA3A5Sl-A is the R3 line. These

three lines correspond to the stator outputs of a synchro. The ratio of the voltages on the three output lines for each functional position of ROLL switch 1A3A5S1 is shown in table 2-3.

Table 2-3. ROLL Switch Positions and Corresponding Ratios

ROLL switch 1A3A5S1 position	Ratio of voltages on outputs $\left(\frac{R1-R3}{R1-R2}\right)$
+30	+0.500
+25	+0.424
+20	+0.347
+15	+0.268
+10	+0.185
+5	+0.096
0	0.000 (R1–R3) = (R1–R2)
−5	−0.096
−10	−0.185
−15	−0.268
−20	−0.347
−25	−0.424
−30	−0.500

c. Barometric Altitude Sensor Simulator. BARO ALT potentiometer 1A3R4 receives a reference voltage from the SDC on pin t of SIGNALS connector 1A3J4. A portion of this reference voltage (from zero to +6.2 Vdc) is tapped off through the BARO ALT potentiometer and returned to the SDC on the arm line through pin N of connector 1A3J4. Both of these dc voltages are measured with respect to the ground line from the SDC at pin s of SIGNALS connector 1A3J4. The reference signal level supplied to BARO ALT potentiometer 1A3R4 is accessible across TEST POINTS 10C (voltage +) and 10A (ground). Refer to paragraph 2-3*e* for a functional description of the circuit.

2-10. time of Day Simulators (fig. FO-9 and 2-7)

a. TIME switches 1A3S8–A and –B can be enabled to produce their outputs either by the arrival of a low level $\overline{\text{T1A}}$ pulse from the SDC or from a low level (signal ground) from TIME SET switch 1A3S11.

b. In the inactive state, the circuit produces logic high level outputs from TIME switches 1A-3S8–A and –B. In this state, the $\overline{\text{T1A}}$ input is at high level, and TIME SET switch 1A3S11 is set as shown, producing an open (logic high level) to the input of TIME switches 1A3S8–A and 1A3S8–B.

c. When $\overline{\text{T1A}}$ from the SDC goes to low level, the number dialed on TIME switches 1A3S8–A and –B produces a two level excess-three BCD coding (on the switch output lines) in which a low level output indicates the active state. The $\overline{\text{T1A}}$ input is generated three times per normal cycle, once each for the seconds, minutes, and hours readings as they would be with the avionics equipment with which the SDC is normally interfaced. Since the test set has only two TIME switch dials, it responds with the same number each time it is enabled.

d The operator can enter the time of day outputs by depressing TIME SET switch 1A3S11 at any time. This enables the output of the circuit to be transmitted to the SDG by means of the enabling low level (ground) transferred through TIME SET switch 1A3S11 to TIME switches 1A3S8–A and –B. When TIME SET switch 1A3-S11 is depressed, the $\overline{\text{T1B}}$ output to the SDC (normally at logic low level) rises to a logic high level as long as the switch is depressed.

e. The $\overline{\text{T1A}}$ signal arrives from the SDC via pin L of RHA IN connector 1A3J7 and is applied to the common (C) connections of TIME switches 1A3S8-A and -B. In its normal (inactive) state, TIME SET switch 1A3S11 presents an open (logic high level) to the C connections of TIME switches 1A3S8-A and -B. At the same time it transfers the signal ground to the $\overline{\text{T1B}}$ line through pins 1 and 2 of TIME SET switch 1A3-S11 and pin M of RHA IN connector 1A3J7. When TIME SET switch 1A3S11 is depressed, pins 3 and 4 transfer the signal ground to activate TIME switches 1A3S8-A and -B and also place an open on the T1B output line from pin 1 of switch 1A3S11.

2-11. Exposure Data Simulator (fig. FO-9)

This circuit consists of EXPSR switch 1A3S10-A. When the test set is connected to the SDC, signal ground is applied to the common (C) pin of the EXPSR switch. This enables the switch to produce its outputs on the EXP1, EXP2, and EXP4 lines continually. The outputs, produced in excess three BCD, are in response to the decimal number dialed on the switch.

2-12. Camera Angular Position and IR Filter Simulators (fig. FO-9 and 3-0)

a. KA–76 ANGULAR POSITION switch 1A-3A5S5 transfers signal ground to any one of five functional positions (placarded as 1 through 5; position 3 not wired). The line to which the

ground sign81 is transferred in four of these positions corresponds to an angular position of the KA76 camera, as shown in table 2-4. The lines not carrying the ground signal have +28 Vdc on them, applied through pullup resistors 1A3A5A2-R1 through R4. The four outputs from switch 1A3A5S5 are routed to the SDC through pins Z, a, b and c of connector 1A3A5P4 and pins GG, FF, EE, and DD of SIGNALS connector 1A3J5.

b. IR FILTER switch 1A3A5S6 transfers the +5 Vdc return from its B deck as the activating signal on any one of five lines (placarded as 1 through 5). The A deck of switch 1A3A5S6 transfers +28 Vdc derived from the power supply through pullup resistor 1A3A5A2R5 to the four output lines not selected by the setting of the switch. The outputs of IR FILTER switch 1A3A5S6 are carried to the SDC via connector 1A3A5P4, pins f, g, h, i, and j, and SIGNALS connector 1A3J4, pins a, b, c, d, and e. The IR filter output derived from switch 1A3A5S6-B in position 3 is also connected to connector 1A3J5, pin n as the ZERO angular displacement signal.

2-13. SLAR Signal Simulators (fig. FO-9)

a. SLAR RANGE switch 1A3A5S3 transfers + 28 Vdc from the power supply to any one of three output lines. These lines simulate SLAR ranges of 25, 50, and 99 kilometers. The three output lines are connected to the SDC via pins W, X, and Y of connector 1A3A5P4 and pins, C, B, and A of SIGNALS connector 1A3J4 as the 1RW1, 1RW2, and 1RW3 outputs.

b. SLAR RANGE DELAY switch 1A3A5S2 transfers +28 Vdc from the power supply to any one of seven output lines. These lines simulate SLAR range delays of zero, 10, 20, 30, 40, 50, or 60 kilometers. The corresponding outputs of this circuit are the SLRO through SLR6 signals, which are sent to the SDC.

Table 2-4. KA-76 ANGULAR POSITION Switch Functions

KA-76 ANGULAR POSITION switch setting	Angular position (Depression angle from pitch axis)
1	15 degrees down from left side.
2	30 degrees down from left side.
3	No connection from switch, but corresponds to zero displacement (0° from roll axis).
4	30 degrees down from right side.
5	15 degrees down from right side.

2-14. Navigation Data Simulators (fig. FO-9 and FO-6)

a. The +5 Vdc return (ground) is connected to the common (C) inputs of all six decks of NAVIGATION DATA switch 1A3S9, enabling them to produce their low level active outputs continuously. Each switch deck produces four outputs for a total of 24. These are applied to the circuit elements on INS simulator board 1A3A3 as shown. Each input line generates a signal on a corresponding output line (INS 1 through INS 24).

b. The circuit which produces the navigation data word consists of six of NAVIGATION DATA thumbwheel switches 1A3S9-A through 1A3S9-F, and a group of 24 inverting line drivers (one for each bit) located on INS simulator board 1A3A3.

c. The circuit operates as follows: The decimal number set by the operator on each of the six decks of NAVIGATION DATA switch 1A3S9 (10^0, 10^1, 10^2, 10^3, 10^4, or 10^5) is converted into excess-three BCD signals on the output side of each of the six switch decks. The output of each switch deck is taken on four lines (2^0, 2^1, 2^2, or 2^3) for the decade it represents. On these lines, a logic low level is the active state ; + 5 Vdc (or an open) is the inactive state.

Example: If the decimal number 2 is dialed on NAVIGATION DATA-10^0 Switch 1A3S9-A, the excess-three logic representation of that number is 0101. The outputs on the switch in this case are ground (zero Vdc) on the $2^0 10°$ and $2^2 10^0$ lines and an open on the $2^1 10^0$ and $2^3 10^0$ lines.

d. The outputs of the switch decks are applied to inverting line drivers on INS simulator board 1ASA3. Taking the case outlined in the preceding example, the four outputs of NAVIGATION DATA -10^0 switch 1A3S9 would be applied to line drivers 1A3A3Z2-F, 1A3A3Z2E, 1A3A3Z9-A, and 1A3A329-B. The low levels on the $2^0 10^0$ and $2^2 10^0$ lines activate inverters 1A3A3Z2-F and 1A3A3Z9-A to produce logic high levels (+ 5 Vdc) on the INS1 and INS3 output lines. The opens (logic high levels) on the $2^1 10^0$ and $2^3 10^0$ inputs to inverters 1A3A3Z2-E and 1A3-A3Z9-B cause them to produce logic low level outputs on the INS2 and INS4 output lines to the SDC.

e. **Any number** (0 through 9) selected on **NAVIGATION DA**TA switch 1A3S9 causes the **circuit to function** in a manner similar to that **just described.**

2-15. Display Select Controls
(fig. FO-9④ and FO-7)

a Inputs to this circuit **are the vertical and** horizontal deflection drive **signals, the display** unblanking signals, and the **CRT control and operating voltages from the SDC.**

b. The deflection drive and unblanking signals from the SDC form the display for the KA60-1, **K**A60-2, IR, SLA**R**, KA76, and CDM data. A separate deflection drive signal is used for each of the four deflection plates in CRT 1ASA5A4V1. These are grouped as +vertical deflection, -vertical deflection, + horizontal deflection, and -horizontal deflection drive. The deflection drive **signals** in the four groups specified and the **unblanking** signals are connected to separate decks on DISPLAY SELECT switch 1ASA5S7. Within each of the four **gr**oups of deflection drive signals, there are three separate input lines, one **each for KA**69-1 and KA60-2, and one for the **KA76, I**R, SLAR, and CDM inputs. The same **deflection signals are used in** the SDC test for the **KA76, IR, SLAR and CDM** displays.

c. The +vertical deflection inputs enter the circuit through pins C, A, and B of RHA IN **connector 1A3J**7 and pins C, A, and B of connector **1A3A5J3,** and are applied to DISPLAY **SELECT switch** 1ASA5S7-A. The + horizontal **deflection inputs** enter through pins J, G, and H **of RHA IN connector 1A3J6 and pins K, H, and J of connector 1A3A5J3, and are applied to switch 1A3A5S7–C. The –horizontal deflection inputs enter through pins F, D, and E of RHA IN connector 1A3J7 and pins F, D,** and E of connector **1A3A5J3, and are applied** to switch 1A3A-**5S7–B. The –vertical deflection inputs enter the circuit through pins M, K, and L of connector 1A-3A5PJ3 after being routed through pins N, L, and M of connector 1A3J7 and are then applied to switch 1A3A5S7–D.**

d. **The unblanking signals enter on five separate lines: One each for KA60–1, KA60–2, KA76, and CDM; the remaining line carries either IR or SLAR data. These signals enter through pins T, S, N, B, and R of RHA IN connector J6 and pins T, N, S, B, and R of connector 1A3A5J2. The unblanking signals are then applied to switch 1A3A5S7–E.**

e. DISPLAY SELECT switch **1A**3A5S7 transfers four deflection signals and the unblanking signal from any of the six sources within the SDC. Each of these (KA60-1, KA60-2, SLAR, IR, KA-76, or CDM) represents the **data output from** the SDC that would normally g**o to the display** section of one of these airborne **equipment. Horizontal** deflection (+), horizontal **deflection (–),** vertical deflection (+) and ve**ertical deflection** (-) are transferred to the de**flection p**lates **of** DISPLAY CRT 1ASA5A4V1 d**irectly from DIS**PLAY SELECT switch 1ASA5S7 decks C, B, A, and D, respectively. The selected unblanking signal is applied to the control grid of DI**SPLAY** CRT 1ASA5A4V1 through 1ASA5S7-E **and an** unblanking and intensity control networ**k which** keeps the unblanking signals at the pro**per volt**age level for display. DIM control 1ASR**5 allows** adjustment of the intensity of the di**splay.**

j. The vertical deflection (-), h**orizontal de**flection (-) and unblanking si**gnals used to form** the display on DISPLAY CRT 1A3A5A4V1 a**re** brought to front panel jacks J54, J56, and J57 as the SCOPE Y, SCOPE X, and SCOPE Z outputs, respectively. From these jacks, the display can be formed on an external CRT.

g. When DISPLAY SELECT switch 1ASA5-S7 is set to any of its six function position**s** (placarded as KA60-1, KA69-2, SLAR, IR, KA76, and CDM) it transfers the appropriate deflection drive signals to the deflecting electrodes in DISPLAY cathode ray tube 1ASA5A4V1. Decoupling capacitors 1ASA5A1C1 through Cl2 shunt noise on each line to signal shield ground, return.

h. The unblanking signals are transferred by switch 1ASA5S7-E to the control grid (pin 3) of CRT 1ASA5A4V1 through coupling capacitor 1ASA5C15 and DIM potentiometer 1ASA5R5.

i. The DISPLAY CRT is of the flat-faced, electrostatically focused and deflected type. Its operating and control voltages are as follows : The filament and cathode connections at pins 1 and 2 have approximately +6.3 Vdc across them. The -442 Vdc level from the SDC power supply is applied to the common filament and cathode of CRT 1ASA5AQV1. The -437.5 Vdc filament voltage floats, while the -442 Vdc is referenced to ground. The -522 Vdc from the SDC is applied to the control grid of the CRT through the resistive rework formed by 1ASA5R3, R4, R5 and 1A3A5R5 to establish a -80 Vdc bias which keeps the CRT off. When the +80 Vdc unblanking pulses arrive, this bias is overcome, the CRT

conducts, and a display is formed. The intensity of the display is controlled by the setting of **DIM** control 1ASA5R5.

j. The focusing electrode, pin 4, is biased by the voltage tapped through FOCUS potentiometer 1ASA5R13 and applied through the network formed of resistors 1ASA5R12, R14, R15, and R16. The accelerator anode, pin 7, is biased by the +500 Vdc input from pin X of RHA IN connector 1ASJ6 and connector 1ASA5J2.

2-16. Cycling Rate Controls (fig. FO-9 ④, FO-90⑤, and Z-3).

This circuit consists of CYCLING RATE switch 1A3S1 and potentiometer 1A3RS (part 4) and resistor 1ASR6 (part 5).

a. Potentiometer 1A3R3 has +100 Vdc applied across it from pins 5 and 8 of power supply connector 1ASA1J1 (part 1). The potentiometer taps off a portion of this de voltage and applies it to pin 3 of CYCLING RATE switch 1A3S1. Switch 1A3S1 transfers this voltage to its output line when it is placed at INTERNAL. When it is set at EXTERNAL, switch 1A3S1 transfers the auto/man Vg/H input it receives via SIGNALS connector 1A3J4, pin V, to the output line through pin Z of connector 1A3J4.

b. Resistor 1A3R6 (fig. FO-9 ④) is a load resistor for placing +28 Vdc from the power sup ply on the out of range Vg/H output line to the SDC through pin X of SIGNALS connector 1A3-J4.

2-17. System Lamp Test, Frame Reset, and Mode Control (fig. FO-9 ③ and 2-9)

a. The circuit is made up of SYSTEM TEST switch 1A3S13, SYSTEM LAMP TEST NO GO indicator 1ASDS7, FRAME NO RESET switch 1A3S12, MODE SEL switch 1A3S14, and resistors 1ASA4R11 and 1ASA4R12.

b. In its normal, inactive, position SYSTEM TEST switch 1A3S13 transfers a logic low level (ground) on the test output line and a logic **high** level (+5 Vdc) on the test output line. **When** depressed to initiate a go/no-go test within the SDC, SYSTE**M** TEST switch 1A3S13 transfers a logic high level on the test line and a logic low level to the test line. The go/no-go input to system lamp test is at high level both in the inactive state and when the system test indicates a go condition. In such a case, SYSTEM LAMP TEST NO GO indicator 1A3DS7 remains off, since it has +5 Vdc at both terminals. If the system test is no-go, the go/no-go input goes to low level, lighting NO GO indicator 1A3DS7.

c. FRAME NO RESET switch 1A3Sl2 is used to generate the low level frame count reset signal to the SDC, and also to provide a self check path for lighting NO GO indicator 1A3DS7, when depressed.

d. MODE SEL switch 1A3S14 has three positions, each of which cause the SDC to produce different display outputs. When set to BCD, MODE SEL switch 1A3S14 places a logic low level on the BCD output line, causing the SDC to produce BCD dot patterns for display on the DISPLAY CRT in the test set. When set to NUM, switch 1A3S14 transfers a low level to the numeric output line, causing the SDC to produce display driver signals for arabic numerals. When switch 1A3S14 is at ATLN, logic high levels (open circuits) are on both the BCD and numeric lines, causing the SDC to produce display drive signals alternating between the BCD and the numeric type.

2-18. Power Supply (fig. FO-9 ①)

a. AC Power. The power supply distributes 115 Vac, 400 Hz primary power to the SDC and produces 26 Vac, 400 Hz power which is distributed to the SDC and to circuits within the test set. Single-phase 115 Vac, 400 Hz power from an external source is applied to circuit breaker 1A3CB2. When the circuit breaker is set to ON, the 115 Vac and its return is applied across ELAPSED TIME meter 1A3M1 to start it. The 115 Vac lines are then distributed to the SDC through POWER OUT connector 1A3J2 and also placed across filters 1A3FL3 and 1A3-FL4. The filtered 115 Vac lights 115 Vac lamp 1A3DS3 and is applied across the primary of transformer 1A3A1T1. The three secondary windings of transformer 1A3A1T1 tap off portions of the primary ac voltage to power the test set dc power supplies and to develop a 26 Vac output. The 26 Vac is tapped from terminals 5 and 6 of 1A3A1T1, and it is used to light POWER 26 Vac lamp 1A3DS4 before it is applied to the primaries of transformers 1A3A5T1 and 1A3A5-T2 within the test set.

b. DC Power. The ac voltage from terminals 7 and 8 of the secondary of transformer 1A3-

A1T1 is applied to the bridge rectifier made UP of diodes 1A3A1CR5, CR6, CR7, and CR8. The output of the bridge rectifier, a dc voltage of approximately +140 Vdc, is filtered by the filter network. When 100 VDC ON-OFF circuit breaker 1A3CB4 is set to ON, this voltage is applied across the voltage regulator made up of resistor 1A3A1R8 and Zener diode 1A3A1VR1. These two elements insure that a constant +100 Vdc is dropped across them to the +100 Vdc return. The +100 Vdc output lights POWER 100 VDC indicator lamp 1A3DS6. and is applied to potentiometer 1A3R3 in the cycling rate controls.

(1) *+28 Vdc power circuit.* When 28 VDC ON-OFF circuit breaker 1A3CB1 is set to ON, +28 Vdc and its return from the external power supply is applied through filters 1A3FL1 and 1A3FL2 across POWER 28 VDC indicator lamp 1A3DS2, thereby lighting it. The filtered +28 Vdc goes to the data demand controls to the SDC power relay return line and through filter 1A3FL5. If the power relay has been energized in the SDC, the connection through the return line from the SDC is made and RELAY RTN indicator lamp 1A3DS1 lights.

(2) +5 V& power supply. The +5 Vdc power supply is the regulated source of operating power for all the integrated circuit elements and the 5 VDC POWER ON lamp within the test set as well as for the battery simulator.

(a) AC voltage from the secondary of transformer 1A3A1T1 is impressed across the bridge rectifier made up of diodes 1A3A1CR1, CR2, CR3, and CR4. The dc output of the bridge rectifier is applied to voltage regulator 1A3A1Z1 and power pass transistor 1A3A1Q1 through filter capacitors 1ASA1C7 and C9, when POWER 5 VDC ON-OFF circuit breaker is set to ON.

NOTE

Voltage regulator 1A3A1Z1 is an integrated circuit micro element.

(*b*) The filtered dc output from the bridge rectifier is sent through circuit breaker 1A3CB3, from which enters voltage regulator 1ASA1VR1 through its E, input. The second input to the voltage comparator is a sample of the output of the +5 Vdc power supply which is fed back from resistor 1ASA1R4 through FB and E. inputs to voltage regulator 1A3A1Z1. Any change in voltage output of the power supply is thus reflected in the sample fed back to the voltage comparator. This change causes a corresponding change in the base drive output to power pass transistor 1A3A1Q1, causing a compensating change in the output of the +5 Vdc power supply.

(c) Changes in current are similarly compensated for by the regulator from the sample taken through resistor 1A3A1R4. Feedback current limit potentiometer 1A3A147 allows adjustment of this function.

(d) The regulated +5 Vdc output is taken across decoupling capacitor 1ASA1C12. Zener diode clamp 1A3A1VR2 protects against voltage spikes in the line. The presence of a 5 Vdc output lights +5 VDC indicator lamp 1ASDS5. The regulated +5 Vdc output is applied to circuit elements within the test set and through blocking diode 1A3CR1 to the battery simulator in the SDC. When the +5 Vdc power supply which supplies the clock circuits in the SDC is operating properly, the +5 Vdc power supply in the test set sinks current through diode CR1. When the +5 Vdc power supply in the SDC is inoperative, the +5 Vdc power supply in the test set supplies approximately + 4.8 Vdc at 0 5 ampere to the clock circuits in the SDC.

CHAPTER 3

GENERAL SUPPORT MAINTENANCE

Section I. General

3-1. Scope

The maintenance duties assigned to general support maintenance for the SDC test set are listed below. Next to each entry in this list is a reference to a paragraph giving detailed information on each maintenance function.

a. Troubleshooting (para 3-3).

b. Removal and replacement (para 3-12 and S-13).

c. Alignment and adjustment (para 3-14).

d. Repair (para 3-21).

e. Performance testing (para 2-24).

3-2. Tools, Test Equipment, and Materials Required

Special tools, test equipment, and materials required for maintenance as follows :

a. Tools and Test Equipment. The tools and test equipment listed in table 3-l are required to perform general support maintenance functions.

b. Special Too&. Special tools required are listed in table 3-2.

c. Materials. Cleaning compound (FSN 7930-395-9542) is required for cleaning equipment and electrical contacts.

WARNING

Prolonged breathing of cleaning compound is dangerous; provide adequate ventilation. Cleaning compound is flammable; do not use near an open flame.

Tab& S-l. Toots and Test Equipment

Item
Tool Kit TK-100/G
Tool Kit TK-105/G
Multimeter TS-352B/U
Oscilloscope AN/USM-281A
Voltmeter ME-202B/U
Ratio Transformer TF-515/U
Pulse Generator (HP-214A)
Test Set, Control Monitor-&cording Head AN/AYM-9
Resistor, 390 ohms ±5 percent, 1 watt (RCR32G391JR)

Table S-Z. Special Tools

Tool or device
Positioner, Buchanan No. 4716-2
Crimper, Buchanan No. 11743
Inserter, Transitron Electronics Co., PCD91-023
Extractor, Transitron Electronics Co., PCD91-021
Positioner, Buchanan No. 4551-l
Positioner, Buchanan No. 4561-2
Crimper, AMP No. 59250 Red & Blue Stake-On
Positioner, MS 3191-20A
Positioner, MS 3191-16A

Section II. GENERAL SUPPORT TROUBLESHOOTING

3-3. General

Troubleshooting of the SDC test set is based on the performance test (para 3-24). To troubleshoot the equipment, perform the procedures of this test, step-by-step, until an abnormal condition or result appears. When this happens, note the step in which you first noticed the abnormality and turn to the corresponding item number in the troubleshooting chart (para 3-4). Perform the checks and corrective actions indicated in the troubleshooting chart If the corrective actions indicated do not correct the trouble, refer the equipment to depot maintenance. The remaining paragraphs in this section contain useful information for performing troubleshooting check and corrective actions, such as-

a. Interior and exterior visual inspection (para 3-5.

b. Voltage and resistance measurements (para 3-6).

c. Waveforms (para 3-7).

d. Continuity checks (para 3-8).

e. Test points location (pars 3-9).

f. Parts location (para 3-10).

g. System wiring and interconnection (pars S-11).

3-4. Troubleshooting Chart

The troubleshooting chart is table 3-3. Note that the chart is divided into four columns. Item No. refers to the step in the performance teat (para 3-24) in which the trouble would first appear. Under the Symptom heading are listed the abnormal indications you might observe or note. Under Probable trouble is listed the possible cause or causes of the trouble. *Corrective action* gives you directions for remedying the trouble. The action may be as simple as a visual check or it may be a reference to a paragraph which gives you test procedures. In any case, the corrective action given is one for which you have the proper tools and test equipment at the general support level. If there is no corrective action within the scope of your duties, you will be directed to refer the equipment to depot maintenance.

Table d-8. Troubleshooting Chart

Item No.	Symptom	Probable trouble	Corrective action
1	Cable continuity does not check.	Wiring defective.	Replace defective cable (fig. FO-10).
2	a. 115VAC POWER lamp and 26VAC POWER lamp do not light and ELAPSED TIME meter does not run.	a.	a.
		(1) External power source defective.	(1) Perform voltage check of external power source. Replace external source if defective.
		(2) Cable 2W8 defective.	(2) Replace cable 2W8.
		(3) 115VAC POWER circuit breaker 1A3CB2 defective.	(3) Perform continuity check of circuit breaker 1A3CB2 (para 3-8). Replace if defective.
	b. 115VAC POWER lamp does not light.	b.	b.
		(1) Housing 1A3XDS3 defective.	(1) Perform continuity check of housing 1A3XDS3 (para 3-8). Replace if defective.
		(2) Filter 1A3FL3 or 1A3FL4 defective.	(2) Perform continuity check of filters 1A3FL3 and 1A3FL4 (para 3-8). Replace if defective.
		(3) Wiring defective.	(3) Perform continuity check of wiring (para 3-8). Replace if defective.
	c. 26VAC POWER lamp does not light.	c.	c.
		(1) Transformer 1A3A1T1 defective.	(1) Perform voltage measurement on transformer 1A3A1T1 (para 3-6). Replace if defective.
		(2) Housing 1A3XDS4 defective.	(2) Perform continuity check on housing 1A3XDS4 (para 3-8). Replace if defective.
		(3) Wiring defective.	(3) Perform continuity check of wiring (para 3-8). Replace if defective.
	d. ELAPSED TIME meter does not operate.	d.	d.
		(1) ELAPSED TIME meter 1A3M1 defective.	(1) Check voltage across ELAPSED TIME meter 1A3M1 (para 3-6). Replace meter 1A3M1 if voltage is correct.
		(2) Wiring defective.	(2) Perform continuity check of wiring (para 3-8). Replace if defective.

Item No.	Symptom	Probable trouble	Corrective action
3	28VDC power lamp does not light.	a. External power source defective.	a. Check output voltage of external 28 Vdc power source. Replace if defective.
		b. Cable 2W8 defective.	b. Replace cable 2W8.
		c. Circuit breaker 1A3CB1 defective.	c. Perform continuity check of circuit breaker 1A3CB1 (para 3–8). Replace if defective.
		d. Filter 1A3FL1 or 1A3FL2 defective.	d. Perform continuity check of filters 1A3FL1 and 1A3FL2 (para 3–8). Replace if defective.
		e. Housing 1A3XDS2 defective.	e. Perform continuity check of housing 1A3XDS2 (para 3–8). Replace if defective.
		f. Wiring defective.	f. Perform continuity check of wiring (para 3–8). Replace if defective.
4	100VDC POWER lamp does not light.	a. Zener diode 1A3A1VR1 defective.	a. Check resistance of Zener diode 1A3A1VR1 (para 3–6). Replace if defective.
		b. Resistor 1A3A1R8 defective.	b. Check resistance of resistor 1A3A1R8 (para 3–6). Replace if defective.
		c. Resistor 1A3A1R5 defective.	c. Check resistance of resistor 1A3A1R5 (para 3–6). Replace if defective.
		d. Inductor 1A3A1L1 defective.	d. Check resistance of inductor 1A3A1L1 (para 3–6). Replace if defective.
		e. Capacitor 1A3A1C10 defective.	e. Check voltage across capacitor 1A3A1C10 (para 3–6). Replace if defective.
		f. Capacitor 1A3A1C11 defective.	f. Check voltage across capacitor 1A3A1C11 (para 3–6). Replace if defective.
		g. Capacitor 1A3A1C13 defective.	g. Check voltage across capacitor 1A3A1C13 (para 3–6). Replace if defective.
		h. Bridge rectifier 1A3A1CR5, 1A3A1CR6, 1A3A1CR7, and 1A3A1CR8 defective.	h. Perform voltage measurement of diodes 1A3A1CR5, 1A3A1CR6, 1A3A1CR7, 1A-3A1CR8 and associated stage parts (para 3–6). Replace if defective.
		i. Transformer 1A3A1T1 defective.	i. Perform resistance measurements on transformer 1A3A-A1T1 (para 3–6). Replace if defective.
		j. Housing 1A3XDS6 defective.	j. Perform continuity check of housing 1A3XDS6 (para 3–8). Replace if defective.
		k. Wiring defective.	k. Perform continuity check of wiring. Replace if defective.
5	5 VDC POWER lamp does not light.	a. Zener diode 1A3A1VR2 defective.	a. Check resistance of Zener diode 1A3A1VR2 (para 3–6). Replace if defective.
		b. Resistor 1A3A1R4 defective.	b. Check resistance of resistor 1A3A1R4 (para 3–6). Replace if defective.
		c. Transistor 1A3A1Q1 defective.	c. Perform voltage and resistance measurements on transistor 1A3A1Q1 (para 3–6). Replace if defective.

Item No.	Symptom	Probable trouble	Corrective action
		d. Capacitor 1A3A1C12 defective.	d. Check voltage across capacitor 1A3A1C12 (para 3-6). Replace if defective.
		e. Resistor 1A3A1R6 defective.	e. Check resistance of resistor 1A3A1R6 (para 3-6). Replace if defective.
		f. Potentiometer 1A3A1R7 defective.	f. Perform resistance measurement of potentiometer 1A3A1R7 (para 3-6). Replace if defective.
		g. Filter capacitors 1A3A1C7 and 1A3A1C9 are defective.	g. Perform voltage measurements of capacitors 1A3A1C7 and 1A3A1C9 (para 3-6). Replace if defective.
		h. Bridge rectifier consisting of 1A3A1CR1, 1A3A1CR2, 1A2A1CR3, and 1A3A1CR4, is defective.	h. Perform voltage measurements on bridge rectifier diodes (para 3-6). Replace if defective.
		i. Transformer 1A3A1T1 is defective.	i. Perform voltage measurements on transformer 1A3A1T1 (para 3-6). Replace if defective.
		j. Voltage regulator 1A3A1Z1 defective.	j. Replace voltage regulator 1A3A1Z1.
		k. Wiring defective.	k. Perform continuity check of wiring (para 3-8). Replace if defective.
6	a. Incorrect voltage readings at TEST POINTS 12C, 12A, 12B, OR 12D, when NAVIGATION DATA 10° switch is set.	a. (1) NAVIGATION DATA 10^0 switch 1A3S9-A defective. (2) INS simulator board 1A3A3 defective. (3) Wiring defective.	a. (1) Check continuity of switch 1A3S9-A (para 3-8). Replace if defective. (2) Replace INS simulator board 1A3A3. (3) Perform continuity check of wiring (para 3-8). Replace if defective.
	b. Incorrect voltage readings at TEST POINTS 13C, 13A, 13B OR 13D, when NAVIGATION DATA 10° switch is set.	b. (1) NAVIGATION DATA 10^1 switch 1A3S9-B defective. (2) INS simulator board 1A3A3 defective. (3) Wiring defective.	b. (1) Check continuity of switch 1A3S9-B (para 3-8). Replace if defective. (2) Replace INS simulator board 1A3A3. (3) Perform continuity of wiring (para 3-8). Replace if defective.
	c. Incorrect voltage readings at TEST POINTS 14C, 14A, 14B, OR 14D, when NAVIGATION DATA 10° switch is set.	c. (1) NAVIGATION DATA 10^2 switch 1A3S9-C defective. (2) INS simulator board 1A3A3 defective. (3) Wiring defective.	c. (1) Check continuity of switch 1A3S9-C (para 3-8). Replace if defective. (2) Replace INS simulator board 1A3A3. (3) Perform continuity check of wiring (para 3-8). Replace if defective.
	d. Incorrect voltage readings at TEST POINTS 15C, 15A, 15B, or 15d, when NAVIGATION DATA 10° switch is set.	d. (1) NAVIGATION DATA 10^3 switch 1A3S9-D defective. (2) INS simulator board 1A3A3 defective. (3) Wiring defective.	d. (1) Check continuity of switch 1A3S9-D (para 3-8). Replace if defective. (2) Replace INS simulator board 1A3A3. (3) Perform continuity check of wiring (para 3-8). Replace if defective.

Item No.	Symptom	Probable trouble	Corrective action
	e. Incorrect voltage readings at TEST POINTS 16C, 16A, 16B, OR 16D, when NAVIGATION DATA 10° switch is set.	e. (1) NAVIGATION DATA 10° switch 1A3S9–E defective. (2) INS simulator board 1A3A3 defective. (3) Wiring defective.	e. (1) Check continuity of switch 1A3S9–E (para 3–8). Replace if defective. (2) Replace INS simulator board 1A3A3. (3) Perform continuity check of wiring (para 3–8). Replace if defective.
	f. Incorrect voltage readings at TEST POINTS 17C, 17A, 17B, OR 17D, when NAVIGATION DATA 10° switch is set.	f. (1) NAVIGATION DATA 10° switch 1A3S9–F is defective. (2) INS simulator board 1A3A3 defective. (3) Wiring defective.	f. (1) Check continuity of switch 1A3A9–F (para 3–8). Replace if defective. (2) Replace INS simulator board 1A3A3. (3) Perform continuity check of wiring (para 3–8). Replace if defective.
7	a. Incorrect voltage readings at pins e, Y, b or h of J3, when FOCAL LENGHT (units) switch dial is set.	a. (1) FOCAL LENGTH (units) switch 1A3S8–C defective. (2) Display and data demand board 1A3A2 defective. (3) Wiring defective.	a. (1) Perform continuity check of switch 1A3S8–C (para 3–8). Replace if defective. (2) Replace defective display and data demand board 1A3A2. (3) Perform continuity check of wiring (para 3–8). Replace if defective.
	b. Incorrect voltage readings at pins a, Y, b or h of connector when FOCAL LENGTH (tens) switch dial is set/	b. (1) FOCAL LENGTH (tens) switch 1A3S8–D defective. (2) Display and data demand board 1A3A2 defective. (3) Wiring defective.	b. (1) Perform continuity check of switch 1A3S8–D (para 3–8). Replace if defective. (2) Replace display and data demand board 1A3A2. (3) Perform continuity check of wiring (para 3–8). Replace if defective.
8	Incorrect KA60 DATA DEMAND waveshape (fig. 3-1) at pin v of connector 1A3J5, with DATA DEMAND KA-60 switch at CONTINUOUS DISPLAY and PRIORITY switch at KA60-1.	a. Defective PRIORITY switch 1A3S7.	a. Perform continuity check of PRIORITY switch 1A3S7 (para 3–8). Replace if defective.
		b. Display and data demand board 1A3A2 defective.	b. Replace defectve display and data demand board 1A3A2 (fig. 3–11).
		c. Integrated circuit 1A3Z1 defective.	c. Replace defective integrated circuit 1A3Z1 (fig. 3–11).
		d. Defective DATA DEMAND KA–60 switch 1A3S5.	d. Perform continuity check of DATA DEMAND KA–60 switch 1A3S5 (para 3–8). Replace if defective.
		e. Wiring defective.	e. Perform continuity check of wiring (para 3–8). Replace if defective.
9	Incorrect KA60 DATA DEMAND waveshape (fig 3-1) at pin v of connector 1A2J5, with PRIORITY switch at KA60-1 and DATA DEMAND KA-60 switch at SINGLE PULSE, when PULSE switch is momentarlly depressed.	a. Defective PULSE switch 1A3S6.	a. Perform continuity check of PULSE switch 1A3S6 (para 3–8). Replace f defective.
		b. Same as item 8.	b. Same as item 8.

Item No.	Symptom	Probable trouble	Corrective action
10	Incorrect KA60 DATA DEMAND swaveshape (fig. 3-1) at pin x of connector 1A3J5, with PRIORITY swtitch at KA60-2 and DATA D E M A N D SINGLE PULSE, when PULSE switch is monentraily depressed.	Same as item 9.	Same as item 9.
11	Incorrect KA60 DATA DEMAND waveshape (fig. 3-1) at pin x of connector 1A3J5, with PRIORITY switch at KA60-2 and DATA DEMAND KA-60 switch at CONTINUOUS DISPLAY.	Same as item 8.	Same as item 8.
12	Incorrect IR DATA DEMAND waveshape at TEST POINT 9A, (fig. 3-1) with DATA DEMAND IR switch at CONTINUOUS DISPLAY.	*a.* Display and data demand board 1A3A2 defective. *b.* Defeective DATA DEMAND IR switch 1A3S2. *c.* Wiring defective.	*a.* Replace defective display and data demand board 1A3A2. *b.* Perform continuity check of IR DATA DEMAND switch 1A3S2 (para 3-8). Replace if defective. *c.* Perform continuity check of of wiring (para 3-8). Replace if defective.
13	Incorrect IR DATA DEMAND waveshape at TEST POINT 9A (fig. 3-1) with DATA DEMAND IR switch at SINGLE PULSE, when PULSE switch is momentarily depressed.	*a.* Defective PULSE switch 1A3S6. *b.* Same as item 12.	*a.* Perform continuity check of PULSE switch 1A3S6 (para 3-8). Replace if defective. *b.* Same as item 12.
14	Incorrect SLAR DATA DEMAND waveshape (fig. 3-1) at TEST POINT 9B, with DATA DEMAND-SLAR switch at CONTINUOUS DISPLAY.	*a.* Display and data demand board 1A3A2 defective. *b.* SLAR DATA DEMAND switch 1A3S3 defective. *c.* Wiring defective.	*a.* Replace defective display and data demand board 1A3A2. *b.* Perform continuity check of SLAR DATA DEMAND switch 1A3S3 (para 3-8). Replace if defective. *c.* Perform continuity check of wiring (para 3-8). Replace if defective.
15	Incorrect SLAR DATA DEMAND waveshape (fig. 3-1) at TEST POINT 9B with DATA DEMAND SLAR switch at SINGLE PULSE, when PULSE switch is monentarily depressed.	*a.* Defective PULSE switch 1A3S6. *b.* Same as item 14.	*a.* Perform continuity check of PULSE switch 1A3S6 (para 3-8). Replace if defective. *b.* Same as item 14.
16	Incorrect KA76 DATA DEMAND waveshape (fig. 3-1) at TEST POINT 9D, with DATA DEMAND KA-76 switch set at CONTINOUS DISPLAY.	*a.* Display and data demand board 1A3A2 defective. *b.* KA-76 DATA DEMAND switch 1A3S4 defective. *c.* Wiring defective.	*a.* Replace defective display and data demand board 1A3A2. *b.* Perform continuity check of KA-76 DATA DEMAND switch 1A3S4 (para 3-8). Replace if defective. *c.* Perform continuity check of wiring (para 3-8). Replace if defective.
17	Incorrect KA-76 DATA DEMAND waveshape (fig. 3-1) at TEST POINT 9D with DATA DEMAND KA-76 SWITCH SET AT single pulse SWITCH IS momentarily depressed	*a.* PULSE switch 1A3S6 defective. *b.* Same as item 16.	*a.* Perform continuity check of PULSE switch 1A3S6 (para 3-8). Replace if defective. *b.* Same as item 14.
18	Incorrect AL-1, AL-2 and AL-3 waveshape (fig 3-1) at TEST POINTS 11A, 11B and 11C.	*a.* INS simulator board 1A3A3 defective. *b.* Wiring defective.	*a.* Replace defective INS simulator board 1A3A3. *b.* Perform continuity check of wiring (para 3-8). Replace if defective.

Item No.	symptom	Probable trouble	Corrective action
19	a. With DATE-DAY switches set at 40:	a.	a.
	(1) No voltage obtained at pin B of connector 1A3J3.	(1) (a) Resistor 1A3A4R4 defective. (b) Wiring defective.	(1) (a) Check resistance of resistor 1A3A4R4 (para 3-6). Replace if defective. (b) Perform continuity check of wiring (para 3-8). (Replace if defective).
	(2) No voltage obtained at pin C of connector 1A3J3.	(2) (a) Resistor 1A3A4R3 defective. (b) Wiring defective.	(2) (a) Check resistance of resistor 1A3A4R3 (para 3-6). Replace if defective. (b) Perform continuity check of wiring (para 3-8). Replace if defective.
	(3) No voltage obtained at pin D of connector 1A3J3.	(3) (a) Resistor 1A3A4R2 defective. (b) Wiring defective.	(3) (a) Check resistance of resistor 1A3A4R2 (para 3-6). Replace if defective. (b) Perform continuity check of wiring (para 3-8). Replace if defective.
	(4) No voltage obtained at pin E of connector 1A3J3.	(4) (a) Resistor 1A3A4R1 defective. (b) Wiring defective.	(4) (a) Check resistance of resistor 1A3A4R1 (para 3-6). Replace if defective. (b) Perform continuity check of wiring (para 3-8). Replace if defective.
	(5) No voltage obtained at pin F of connector 1A3J3.	(5) (a) Resistor 1A3A4R5 defective. (b) Wiring defective.	(5) (a) Check resistance of resistor 1A3A4R5 (para 3-6). Replace if defective. (b) Perform continuity check of wiring (para 3-8). Replace if defective.
	(6) No voltage obtained at pin G of connector 1A3J3.	(6) (a) Resistor 1A3A4R6 defective. (b) Wiring defective.	(6) (a) Check resistance of resistor 1A3A4R6 (para 3-6). Replace if defective. (b) Perform continuity check of wiring (para 3-8). Replace if defective.
	(7) No voltage obtained at pin H of connector 1A3J3.	(7) (a) Resistor 1A3A4R7 defective. (b) Wiring defective.	(7) (a) Check resistance of resistor 1A3A4R7 (para 3-6). Replace if defective. (b) Perform continuity check of wiring (para 3-8). Replace if defective.

Item No.	Symptom	Probable trouble	Corrective action
	(8) No voltage obtained at pin J of connector 1A3J3.	(8) (a) Resistor 1A3A4R8 defective.	(8) (a) Check resistance of resistor 1A3A4R8 (para 3-6). Replace if defective.
		(b) Wiring defective.	(b) Perform continuity check of wiring (para 3-8). Replace if defective.
	(9) No voltage obtained at pin K of connector 1A3J3.	(9) (a) Resistor 1A3A4R9 defective.	(9) (a) Check resistance of resistor 1A3A4R9 (para 3-6). Replace if defective.
		(b) Wiring defective.	(b) Perform continuity check of wiring (para 3-8). Replace if defective.
	(10) No voltage at pin L of connector 1A3J3.	(10) (a) Resistor 1A3A4R10 defective.	(10) (a) Check resistance of resistor 1A3A4R10 (para 3-6). Replace if defective.
		(b) Wiring defective.	(b) Perform continuity check of wiring (para 3-8). Replace if defective.
19	b. with DATE-DAY switches at 00, voltage obtained to pin B of connector 1A3J3 is not zero Vdc.	b. (1) DATE-DAY switch 1A3S10-G defective.	b. (1) Perform continuity check check of DATE-DAY switch 1A3S10-G (para 3-8). Replace if defective.
		(2) Wiring defective.	(2) Perform continuity check of wiring (para 3-8). Replace if defective.
	c. With DATE-DAY switches at 10, voltage obtained at pin C of connector 1A3J3 is not zero Vdc.	c. (1) DATE-DAY switch 1A3S10-G defective. (2) Wiring defective.	c. Same as item 19b.
	d. With DATE-DAY switches at 20, voltage obtained at pin D of connector 1A3J3 is not zero Vdc.	d. (1) DATE-DAY switch 1A3S10-G defective. (2) Wiring defective.	d. Same as item 19b.
	e. With DATE-DAY switches at 30, voltage obtained at pin E of connector 1A3J3 is not zero Vdc.	e. (1) DATE-DAY switch 1A3S10-G defective. (2) Wiring defective.	e. Same as item 19b.
	f. With DATE-DAY switches at 00, voltage obtained at pin B of connector 1A3J3 is not zero Vdc.	f. (1) DATE-DAY switch 1A3S10-F defective.	f. (1) Perform continuity check of DATE-DAY switch 1A3S10-F (para 3-8). Replace if defective.
		(2) Wiring defective.	(2) Perform continuity check of wiring (para 3-8). Replace if defective.
	g. With DATE-DAY switches at 01, voltage obtained at pin C of connector 1A3J3 is not zero Vdc.	g. (1) DATE-DAY switch 1A3S10-F defective. (2) Wiring defective.	g. Same as item 19f.
	h. With DATE-DAY switches at 02, voltage obtained at pin D of connector 1A3J3 is not zero Vdc.	h. (1) DATE-DAY switch 1A3S10-F defective. (2) Wiring defective.	h. Same as item 19f.

Item No.	symptom	Probable trouble	Corrective action
	i. With DATE-DAY switches at 03, voltage obtained at pin E of connector 1A3J3 is not zero Vdc.	i. (1) DATE-DAY switch 1A3S10–F defective. (2) Wiring defective.	i. Same as item 19*f*.
	j. With DATE-DAY switches at 04, voltage obtained at pin F of connector 1A3J3 is not zero Vdc.	j. (1) DATE-DAY switch 1A3S10–F defective. (2) Wiring defective.	j. Same as item 19*f*.
	k. With DATE-DAY switches at 05, voltage obtained at pin G of connector 1A3J3. in not zero Vdc.	k. (1) DATE-DAY switch 1A3S10–F defective. (2) Wiring defective.	k. Same as item 19*f*.
	l. With DATE-DAY switches at 06, voltage obtained at pin H of connector 1A3J3 is not zero Vdc.	l. (1) DATE-DAY switch 1A3S10–F defective. (2) Wiring defective.	l. Same as item 19*f*.
	m. With DATE-DAY switches at 07, voltage obtained at pin J of connector 1A33J3 is not zero Vdc.	m. (1) DATE-DAY switch 1A3S10–F defective. (2) Wiring defective.	m. Same as item 19*f*.
	n. with DATE-DAY switches at 06, voltage obtained at pin k of connector 1A3J3 is not zero Vdc.	n. (1) DATE-DAY switch 1A3S10–F defective. (2) Wiring defective.	n. Same as item 19*f*.
	o. With DATE-DAY switches at 09, voltage obtained at pin L of connector 1A3J3 is not zero Vdc.	o. (1) DATE-DAY switch 1A3S10–F defective. (2) Wiring defective.	o. Same as item 19*f*.
20	a. Incorrect voltage at pins B and C of connector 1A3J3 DATE-MONTH switches set at 00 or 10.	a. Defective DATE-MONTH (tens) switch 1A3S10–E.	a. Check continuity of switch 1A3S10–E (para 3–8). Replace if defective.
	b. Incorrect voltage at pins B through L of connector 1A3J3 with DATE-MONTH switches set at 00, 01, 02, 03, 04, 05, 06, 07, 08, or 09.	b. Defective DATE-MONTH (units) switch 1A3S10–D.	b. Check continuity of switch 1A3S10–D (para 3–8). Replace if defective.
21	a. Incorrect voltages at pins B through L of connector 1A3J3 with DATE-YEAR switches set at 00, 10, 20, 30, 40, 50, 60, 70, 80, or90.	a. Defective DATE-YEAR (tens) switch 1A3S10–C.	a. Check continuity of switch 1A3S10–C (para 3–8). Replace if defective.
	b. Incorrect voltage at pins B through L of connector 1A3J3 with DATE-YEAR switches se at 01, 02, 03, 04, 05, 06, 07, 08, or 09.	b. Defective DATE-YEAR (units) switch 1A3S10–B.	b. Check continuity of switch 1A3S10–B (para 3–8). Replace if defective.
22	a. Incorrect voltages at pins B through L of connector 1A3J3 with SORTIE AND TAKING UNIT switches set at 100, 200, 300, 400, 500, 600, 700, 800, or 900.	a. SORTIE AND TAKING UNIT (10^2 and 10^2) switch 1A3S8–G defective.	a. Check continuity of switch 1A3S8–G (para 3–8). Replace if defective.
	b. Incorrect voltages at pins B through L of connector 1A3J3 with SORTIE AND TAKING UNIT switches set at 010, 020, 030, 040, 050, 060, 070, 080, or 090.	b. SORTIE AND TAKING UNIT (10^1 and 10^2) switch 1A3S8–F defective.	b. Check continuity of switch 1A3S8–F (para 3–8). Replace if defective.
	a. Incorrect voltages at pins B through L of connector 1A3J3 with SORTIE AND TAKING	c. SORTIE AND TAKING UNIT (10^0 and 10^1) switch 1A3S8–E defective.	c. Check continuity of switch 1A3S8–E (para 3–8). Replace if defective.

Item No.	Symptom	Probable trouble	Corrective action
	UNIT switches set at 001, 002, 003, 004, 005, 006, 007, 008 or 009.		
23	a. Incorrect voltages at pins, p, m, and n of connector 1A3J3	a. **EXPSR switch 1A3S10–A defective.**	a. **Check switch continuity (para 3–8). Replace if defective.**
	b. Voltage at pin p of connector 1A3J3 is always zero.	b. **Resistor 1A3A4R15 defective.**	b. **Check resistance of resistor 1A3A4R15 (para 3–6). Replace if defective.**
	c. Voltage at pin n of connector 1A3J3 is always zero.	c. **Resistor 1A3A4R14 defective.**	c. **Check resistance of resistor 1A3A4R14 (para 3–6). Replace if defective.**
	d. Voltage at pin m of connector 1A3J3 is always zero.	d. **Resistor 1A3A4R13 defective.**	d. **Check resistance of resistor 1A3A4R13 (para 3–6). Replace if defective.**
24	a. Incorrect resistances measured at pins z, a, c, or d of connector 1A3J3.	a. **TIME (tens) switch 1A3S8–B defective.**	a. **Check continuity of switch 1A3S8–B (para 3–8). Replace if defective.**
	b. Incorrect resistances measured at pins f, g, i, or j of connector 1A3J3.	b. **TIME (units) switch 1A3S8–A defective.**	b. **Check continuity of switch 1A3S8–A (para 3–8). Replace if defective.**
	c. With TIME switches at 55, resistnace measured at pin j of connector 1A3J3 does not change as TIME SET switch is depressed and released.	c. **TIME SET switch 1A3S11 defective.**	c. **Check continuity of switch 1A3S11 (para 3–8). Replace if defective.**
25	a. SYSTEM NO GO lamp does not light when FRAME NO RESET switch is depressed.	a. **FRAME NO RESET switch 1A3S12 defective.**	a. **Check continuity of switch 1A3S12 (para 3–8). Replace if defective.**
	b. SYSTEM NO GO LAMP does not go out when FRAME NO RESET switch is released.	b. **FRAME NO RESET switch 1A3S12 defective.**	b. **Check continuity of switch 1A3S12 (para 3–8). Replace if defective.**
26	a. No voltage obtained at pin V of connector 1A3J7 with TEST switch off.	a. **(1) TEST switch 1A3S13 defective.** **(2) Resistor 1A3A4R12 defective.**	a. **(1) Check continuity of switch 1A3S13 (para 3–8). Replace if defective.** **(2) Check resistance of resistor 1A3A4R12 (para 3–6). Replace if defective.**
	b. No voltage obtained at pin G of connector 1A3J7 with TEST switch depressed.	b. **(1) TEST switch 1A3S13 defective.** **(2) Resistor 1A3A4R11 defective.**	b. **(1) Check continuity of switch 1A3S13 (para 3–8). Replace if defective.** **(2) Check resistance of resistor 1A3A4R11 (para 3–6). Replace if defective.**
27	Improper continuity measurements at pin X or W of connector 1A3J7	**MODE SEL switch 1A3S14 defective.**	**Check continuity of switch 1A3S14 (para 3–8). Replace if defective.**
23	a. Incorrect KA-76 ANGULAR POSITION voltages obtained at pins GG, FF, EE, or DD of connector 1A3J5.	a. **KA–76 ANGULAR POSITION switch 1A3AS5 defective.**	a. **Check continuity of switch 1A3A5S5 (para 3–8). Replace if defective.**
	b. Voltage at pin GG of connector 1A3J5 is always zero.	b. **Resistor 1A3A5A2R4 defective.**	b. **Check resistance of resistor 1A3A5A2R4 (para 3–6). Replace if defective.**
	c. Voltage at pin FF of connector 1A3J5 is always zero.	c. **Resistor 1A3A5A2R3 defective.**	c. **Check resistance of resistor 1A3A5A2R3 (para 3–6). Replace if defective.**
	d. Voltage at pin EE of connector 1A3J5 is always zero.	d. **Resistor 1A3A5A2R2 defective.**	d. **Check resistance of resistor 1A3A5A2R2 (para 3–6). Replace if defective.**

Item No.	Symptom	Probable trouble	Corrective action
	a. Voltage at pin DD of connector 1A3J5 is always zero.	a. Resistor 1A3A5A2R1 defective.	a. Check resistance of resistor 1A3A5A2R1 (para 3–6). Replace if defective.
29	a. Incorrect IR FILTER voltages at pins a, b, c, d, or e of connector 1A3J4 or pin m of connector 1A3J5.	a. IR FILTER switch 1A3A5S6 defective.	a. Check continuity of switch 1A3A5S6 (para 3–8). Replace if defective.
	a. Voltage at pins a, b, c, d, or e of connector 1A3J4 or pin m of connector 1A3J5 is always zero.	b. Resistor 1A3A5A2R5 defective.	b. Check resistance of resistor 1A3A5A2R5 (para 3–6). Replace if defective.
30	Incorrect SLAR RANGE voltage at pins C, B, OR A of connector 1A3J4.	SLAR RANGE switch 1A3A5S3 defective.	Check continuity of switch 1A3A5-S3 (para 3–8). Replace if defective.
31	Incorrect SLAR RANGE DELAY voltages at pins K, J, H, G, F, E, or D of connector 1A3J4.	SLAR RANGE DELAY switch 1A3A5S2 defective.	Check continuity of switch 1A3A5S2 (para 3–8). Replace if defective.
32	a. Incorrect resistance measurements (BARO ALT) between TEST POINTS 10B and 10C.	a. Defective BARO ALT potentiometer 1A3R4.	a. Perform resistance check of potentiometer 1A3R4 (para 3–6). Replace if defective.
	b. Resistance does not decrease as BARO ALT potentiometer is turned counterclockwise.	b. Same as item 32a.	b. Same as item 32a.
	c. Resistance dose not increase as BARO ALT potentiometer is turned clockwise.	c. Same as item 32a.	c. Same as item 32a.
33	a. Voltage is incorrect between TEST POINTS 11D AND 6B, with CYCLING RATE switch at INTERNAL AND CYCLING RATE potentiometer fully clockwise.	a. (1) CYCLING RATE potentiometer 1A3R3 defective. (2) Zener diode 1A3A1VR1 defective. (3) +100 Vdc power supply defective.	a. (1) Check resistance of potentiometer 1A3R3 (para 3–6). Replace if necessary. (2) Check voltage at TEST POINT 11D (para 3–9). If incorrect, replace Zener diode 1A3A1VR1. (3) Return to item 4.
	b. Voltage does not decrease as CYCLING RATE potentiometer is turned counterclockwise.	b. Same as item 33a(1).	b. Same as item 33a(1).
34	Incorrect roll test voltages.	a. ROLL switch 1A3A5S1 defective.	a. Check continuity of switch 1A3A5S1 (para 3–8). Replace if defective.
		b. 26 Vac power supply defective.	b. Check 26 Vac output at TP5A and TP5B. If good, see item 2c.
		c. Roll ratio transformer 1A3A5T1 defective.	c. Replace transformer 1A3A5T1. (fig. 3–14).
35	Incorrect pitch test voltages.	a. PITCH switch 1A3A5S4 defective.	a. Check continuity of switch 1A3A5S4 (para 3–8). Replace if defective.
		b. 26 Vac power supply defective.	b. Check 26 Vac output at TP5A and TP5B. If good, see item 4.
		c. Pitch ratio transformer 1A3A5T2 defective.	c. Replace transformer 1A3A5T2 (fig. 3–14).
36	a. No display on CRT when DISPLAY SELECT switch is at KA60-1. CRT display visible at other switch positions.	a. DISPLAY SELECT switch 1A3A5S7 defective.	a. Check circuit continuity of 1A3A5S7 (para 3–8 and fig. FO–9). Replace if defective.

Item No.	Symptom	Probable trouble	Corrective action
	b. No display on CRT when DISPLAY SELECT switch is at KA60-2. CRT display visible at other switch positions.	b. Same as item 36a.	b. Same as item 36a.
	c. No display on CRT when DISPLAY SELECT switch is at SLAR. CRT display visible at other switch positions.	c. Same as item 36a.	c. Same as item 36a.
	d. No display on CRT when DISPLAY SELECT switch is at KA76. CRT display visible at other switch positions.	d. Same as item 36a.	d. Same as 36a.
	e. No display on CRT when DISPLAY SELECT switch is at CDM. CRT display visible at other switch positions.	e. Same as item 36a.	e. Same as item 36a.
	f. No display on CRT in any position of DISPLAY SELECT switch.	f.	f.
		(1) Improper CRT operating voltages from CM–RH test set.	(1) Check voltages between TEST POINTS 2B, 2C, and 2D and 18A (gnd). If incorrect, replace CM–RH test set.
		(2) Same as item 36a.	(2) Same as item 36a.
		(3) DIM potentiometer 1A3A5R5 defective.	(3) Check continuity of potentiometer 1A3A5R5 (para 3–8). Replace if defective.
		(4) Focus or accelerating anode biasing network defective.	(4) Perform resistance check of resistors 1A3A5R12, R13, R14, R15, and R16 (para 3–6). Replace if defective.
		(5) CRT socket defective.	(5) Check voltages at socket of CRT (para 3–6). If these are good, replace CRT socket (fig. 3–19).
		(6) Defective CRT 1A3A5A4VR1.	(6) Replace CRT 1A3A5A4V1 (fig. 3–19).

3-5. Interior and Exterior Visual Inspection

a. Exterior Inspection. Make the following checks of the exterior of the test set.

(1) Check the case for damage. If such damage is superficial, touch up the case paint as directed in TM 11–6625–2479–12. If the damage is extensive, replace the case (fig. 3–9).

(2) Check for broken, bent, or missing connectors. Replace damaged connectors.

(3) Check for damaged panel switches, lamp holders, or lenses and replace as necessary.

b. Interior Inspection. To check the electronic parts inside the test set, first gain access to the back of panel assembly 1A3 (fig. 3–11). To check the parts inside monitor assembly 1A3A5 you must remove the access panels (fig. 3–18). Once this is done, check for the following:

(1) Loose or broken parts. Replace as necessary.

(2) Damaged printed circuit boards and connectors. Replace as necessary.

(3) Unsoldered or broken connections. Provided these are not on display-data demand board 1A3A2 or INS simulator board 1A3A3, you should attempt to resolder or replace such connections.

3-6. Voltage and Resistance Measurements

Voltage and resistance measurement data for the test set is presented in table 3–4. The *Component* column refers to component being measured. The *From* and *To* columns refer to the points of measurement. The polarity of the test equipment is shown as (+) for positive lead and (−) for negative lead. The *Figure* column refers to an illustration showing the location of the component being measured or measured across. Refer to paragraph 3–2*c* for test equipment. The *Measurement* column states the reading that should be meas-

ured across the component. These measurements are taken when the test set is not interfaced with any other equipment. All measurements are made with the component in circuit, except for those covered by a rate in the table. Front panel test points 5D, 6B, and 6D are jumped together in order to take measurements. Refer to paragraph 3-2c for test equipment.

Table 3-4. Voltage and Resistance Measurements

Component	Points of measurement		Fig. reference	Measurement
	From	To		
1A3A1C10	1A3A1E38(+)	TEST POINT 6B(−)	3-15	+140 to +165 Vdc
1A3A1C11	1A3A1E39(+)	TEST POINT 6B(−)	3-15	+135 to +165 Vdc
1A3A1C12	1A3A1E14(+)	TEST POINT 6B(−)	3-15	+4.5 to +5.5 Vdc
1A3A1C13	1A3A1E22(+)	TEST POINT 6B(−)	3-15	+130 to +160 Vdc
1A3A1C7	1A3A1E6(+)	TEST POINT 6B(−)	3-15	+12 to +16 Vdc
1A3A1C9	1A3A1E11(+)	TEST POINT 6B(−)	3-15	+12 to +16 Vdc
1A3A1Q1	1A3A1E12(+)	TEST POINT 6B(−)	3-15	+10.7 to +16.1 Vdc
1A3A1Q1	1A3A1E17(+)	TEST POINT 6B(−)	3-15	+4.7 to +6.1 Vdc
1A3A1Q1	1A3A1E21(+)	TEST POINT 6B(−)	3-15	+4.7 to +5.7 Vdc
1A3A1T1	1A3A1E1	1A3A1E4	3-15	10 to 12 Vac
1A3A1T1	1A3A1E24	1A3A1E27	3-15	102 to 120 Vac
1A3A5T1	1A3A5T1–1	1A3A5T1–2	3-14	24 to 28 Vac
1A3A5T2	1A3A5T2–1	1A3A5T2–2	3-14	24 to 28 Vac
1A3R1	TEST POINT 5C(+)	TEST POINT 6D(−)	3-11	+25.5 to +29.5 Vdc
1A3R2	TEST POINT 6D(+)	TEST POINT 5D(−)	3-11	0 Vdc
1A3A1Q1	1A3A1E12(+)	1A3A1E17(−)	3-15	400 to 600 ohms
1A3A1Q1	1A3A1E12(+)	TEST POINT 6B(−)	3-15	3.6K to 5.4K ohms
1A3A1Q1	1A3A1E17(+)	1A3A1E12(−)	3-15	3.2K to 4.8K ohms
1A3A1Q1	1A3A1E17(+)	1A3A1E21(−)	3-15	400 to 600 ohms
1A3A1Q1	1A3A1E21(+)	1A3A1E17(−)	3-15	800 to 1.2K ohms
1A3A1Q1	TEST POINT 6B(+)	1A3A1E12(−)	3-15	18K to 26K ohms
1A3A1R4	1A3A1E16	1A3A1E2	3-15	0.45 to 1.00 ohm
1A3A1R5	1A3A1E34	1A3A1E35	3-15	180 to 220 ohms
1A3A1R6	1A3A1E15	1A3A1E20	3-15	420 to 520 ohms
1A3A1R8	1A3A1E36	1A3A1E37	3-15	900 to 1.1K ohms
1A3A1T1	1A3A1E31	1A3A1E33	3-15	8 to 10 ohms
1A3A1T1	1A3A1T1–1	1A3A1T1–2	3-15	1.7 to 2.3 ohms
1A3A1T1	1A3A1T1–5	1A3A1T1–6	3-15	1.7 to 2.3 ohms
1A3A1VR1	1A3A1E37(+)	1A3A1E23(−)	3-15	29 to 31 ohms
1A3A1VR2	1A3A1E13(+)	1A3A1E14(−)	3-15	5.5 to 7.5 ohms
1A3A1VR2	1A3A1E14(+)	1A3A1E13(−)	3-15	8 to 12 ohms
1A3A4R1	1A3A4E1	1A3A4E2	3-13	2.4K to 3K ohms
1A3A4R10	1A3A4E19	1A3A4E20	3-13	2.4K to 3K ohms
1A3A4R11	1A3A4E21	1A3A4E22	3-13	2.4K to 3K ohms
1A3A4R12	1A3A4E23	1A3A4E24	3-13	2.4K to 3K ohms
1A3A4R13	1A3A4E25	1A3A4E26	3-13	2.4K to 3K ohms
1A3A4R14	1A3A4E27	1A3A4E28	3-13	2.4K to 3K ohms
1A3A4R15	1A3A4E29	1A3A4E30	3-13	2.4K to 3K ohms
1A3A4R2	1A3A4E3	1A3A4E4	3-13	2.4K to 3K ohms
1A3A4R3	1A3A4E5	1A3A4E6	3-13	2.4K to 3K ohms
1A3A4R4	1A3A4E7	1A3A4E8	3-13	2.4K to 3K ohms
1A3A4R5	1A3A4E9	1A3A4E10	3-13	2.4K to 3K ohms
1A3A4R6	1A3A4E11	1A3A4E12	3-13	2.4K to 3K ohms
1A3A4R7	1A3A4E13	1A3A4E14	3-13	2.4K to 3K ohms
1A3A4R8	1A3A4E15	1A3A4E16	3-13	2.4K to 3K ohms
1A3A4R9	1A3A4E17	1A3A4E18	3-13	2.4K to 3K ohms
1A3A5A1R10	1A3A5A1E44	1A3A5A1E60	3-20	740K to 820K ohms
1A3A5A1R11	1A3A5A1E43	1A3A5A1E59	3-20	360K to 390K ohms
1A3A5A1R12	1A3A5A1E49	1A3A5A1E65	3-20	460K to 500K ohms
1A3A5A1R13	1A3A5A1E31	1A3A5A1E33	3-20	460K to 500K ohms
1A3A5A1R14	1A3A5A1E48	1A3A5A1E64	3-20	590K to 650K ohms
1A3A5A1R15	1A3A5A1E47	1A3A5A1E63	3-20	510K to 630K ohms
1A3A5A1R16	1A3A5A1E46	1A3A5A1E62	3-20	580K to 640K ohms

See footnote at the end of table.

Component	Points of measurement		Fig. reference	Measurement
	From	To		
1A3A5A1R17	1A3A5A1E66	1A3A5A1E68	3-20	475 to 525 ohms
1A3A5A1R18	1A3A5A1E67	1A3A5A1E69	3-20	9K to 11K ohms
1A3A5A1R3	1A3A5A1E39	1A3A5A1E55	3-20	780K to 860K ohms
1A3A5A1R4	1A3A5A1E38	1A3A5A1E54	3-20	780K to 860K ohms
1A3A5A1R5	1A3A5A1E37	1A3A5A1E53	3-20	370K to 410K ohms
1A3A5A1R6	1A3A5A1E42	1A3A5A1E58	3-20	700K to 780K ohms
1A3A5A1R7	1A3A5A1E41	1A3A5A1E57	3-20	710K to 790K ohms
1A3A5A1R8	1A3A5A1E40	1A3A5A1E56	3-20	360K to 390K ohms
1A3A5A1R9	1A3A5A1E45	1A4A5A1E61	3-20	740K to 820K ohms
1A3A5A2R1	1A3A5A2E3	1A3A5A2E4	3-21	2K to 2.4K ohms
1A3A5A2R2	1A3A5A2E5	1A3A5A2E6	3-21	2K to 2.4K ohms
1A3A5A2R3	1A3A5A2E7	1A3A5A2E8	3-21	2K to 2.4K ohms
1A3A5A2R4	1A3A5A2E9	1A3A5A2E10	3-21	2K to 2.4K ohms
1A3A5A2R5	1A3A5A2E11	1A3A5A2E12	3-21	270 to 330 ohms
1A3CR1	1A3J7-N(−)	TEST POINT 6A(+)	3-11	Infinite ohms[2]
1A3CR1	TEST POINT 6A (−)	1A3J7-N(+)	3-11	900 to 1.2K ohms
[3]1A3M1	1A3J2-A	1A3J2-B	3-11	5K to 7K ohms
[4]1A3R1	1A3E6	1A3R1	3-11	460K to 560K ohms
[5]1A3R2	1A3E6	1A3R2	3-11	460K to 560K ohms
[6]1A3R3	TEST POINT 10D(+)	TEST POINT 6B(−)	3-11	0 to 5K ohms
[7]1A3R4	TEST POINT 10A	TEST POINT 10B	3-11	0 to 5K ohms
[8]1A3R5	1A3E1	1A3E2	3-11	0 to 250K ohms
1A3R6	TEST POINT 5C	TEST POINT 7A	3-11	5.6K to 6.8K ohms

CYCLING RATE potentiometer fully clockwise.
[2]Greater or equal to 5 Megohms.
[3]Disconnect 1A3A1J1 and 115 VAC indicator lamp 1ASDS3.
[4]Unsolder 1A3R1 lead at 1ASE4.
[5]Unsolder 1A3R2 lead at 1ASE7.
Disconnect 1A3A1P1 from power supply 1A8A1 and vary CYCLING RATE potentiometer from counterclockwise to clockwise position.
Vary BARO ALT potentiometer from counterclockwise to clockwise position.
[8]Unsolder one lead of 1A3ASCR1 and vary potentiometer from counterclockwise to clockwise position.

CAUTION

This equipment has transistorized circuits. Do not use teat instrument8 that are likely to apply excessive vol**tages or** currents through test **leads to transis**tors. When measuring **voltages, use tape** or sleeving to insulate **the entire probe,** except for the extreme tip. A momentary short circuit can ruin the transistor.

3-7. Waveforms

Waveforms for the test set are presented in figure **3–1.** The Preliminary steps **column of figure 3–1** tell13 what action should be **taken before making** measurement. The Point ***of measurement*** **column** refers to point where pro**be** should be connected. All measurements **are** taken with respect to chas**sis ground**. The ***Wav***eforms column shows the **waveform** shape **with** its parameters. Refer to **paragraph** 3-2c for teat equipment.

a. Connect the test set to a 115 Vac, 400 Hz **external** power source and a 28 Vdc external power source as described in TM 11-6625-2479-12 when performing wave **shape analysis.**

b. Jumper front panel TEST POINTS 5D, 6B, and 6D when making measurements.

c. Set all POWER switches to ON.

d. At the conclusion of the measurement, set all PO**WER switches** to O**FF, disconn**ect all **jumper wires, and disco**nnect **all external** power.

3-8. Continuity Checks

Continuity measurements for the teat set switches are presented in table 2-5. This procedure checks continuity of all switches. The Switch column identifies the switch being checked. The Position column refers to the position of switch. The From column refers to one side of switch and the To column refers to other side of switch for continuity.

a. These measurements are taken when the test set is not interfaced with any other equipment. continuity is a resistance measurement

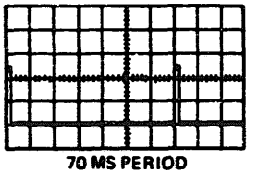
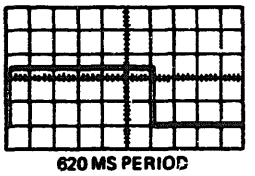
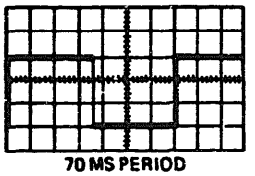
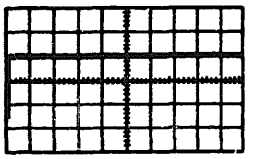
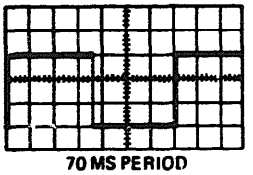
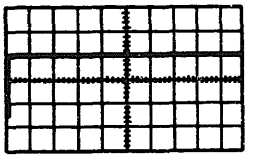
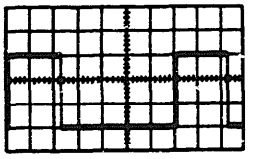
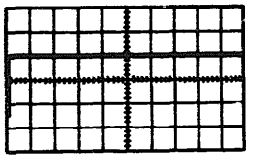
PRELIMINARY STEPS	POINT OF MEASUREMENT (PROBE ON)	WAVEFORMS
Set KA-60 DATA DEMAND switch to CONTINUOUS DISPLAY.	TEST POINT 18D	A  70 MS PERIOD PROBE: 10X VERTICAL: .5V/CM HORIZONTAL: 10 MS/CM SYNC: INT + SWEEP: NORM
Set KA-60 DATA DEMAND switch to SINGLE PULSE and depress PULSE switch.	TEST POINT 18D	B  620 MS PERIOD PROBE: 10X VERTICAL: .5V/CM HORIZONTAL: 100 US/CM SYNC: INT + SWEEP: NORM
Set SLAR DATA DEMAND switch to CONTINUOUS DISPLAY.	TEST POINT 9B	C  70 MS PERIOD PROBE: 10X VERTICAL: 1V/CM HORIZONTAL: 10 MS/CM SYNC: INT + SWEEP: NORM
Set SLAR DATA DEMAND switch to SINGLE PULSE and depress PULSE switch.	TEST POINT 9B	D  PROBE: 10X VERTICAL: 1V/CM HORIZONTAL: 50 US/CM SYNC: INT + SWEEP: NORM
Set IR DATA DEMAND switch to CONTINUOUS DISPLAY.	TEST POINT 9A	E  70 MS PERIOD PROBE: 10X VERTICAL: 1V/CM HORIZONTAL: 10 MS/CM SYNC: INT + SWEEP: NORM
Set IR DATA DEMAND switch to SINGLE PULSE and depress PULSE switch.	TEST POINT 9A	F  PROBE: 10X VERTICAL: 1V/CM HORIZONTAL: 50 US/CM SYNC: INT + SWEEP: NORM
Set KA-76 DATA DEMAND switch to CONTINUOUS DISPLAY.	TEST POINT 9D	G  PROBE: 10X VERTICAL: 1V/CM HORIZONTAL: 10 MS/CM SYNC: INT + SWEEP: NORM
Set KA-76 DATA DEMAND switch to SINGLE PULSE and depress PULSE switch.	TEST POINT	H  PROBE: 10X VERTICAL: 1V/CM HORIZONTAL: 50 US/CM SYNC: INT + SWEEP: NORM

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Figure 3-1. Waveforms.

of less than or equal to 2 ohms. Front panel test points 5D, 6B, and 6D are jumped together. Refer to paragraph 3–2*c* for test equipment.

b. When performing continuity checks from connector 1A3A3J1 or 1A3A2J1, remove circuit boards 1A3A3 or 1A3A2 respectively. Refer to schematic and wiring diagram figures FO–9 through figure FO–17 for supplementary continuity checks.

Table 2-5. Continuity Check Chart

Switch	Position	From	To
		Front panel test points:	Connector 1A3A2J1, pin:
IR DATA DEMAND 1A3S2	CONTINUOUS DISPLAY	6B	1
	SINGLE PULSE	6B	3
SLAR DATA DEMAND 1A3S3	CONTINUOUS DISPLAY	6B	5
	SINGLE PULSE	6B	39
KA–76 DATA DEMAND 1A3S4	CONTINUOUS DISPLAY	6B	4
	SINGLE PULSE	6B	4
KA–60 DATA DEMAND 1A3S5	CONTINUOUS DISPLAY	6B	38
	SINGLE PULSE	6B	6
PULSE 1A3S6	NOT DEPRESSED	6B	47
	DEPRESSED	6B	19
		Front panel test points:	Connector 1A3J7, pin:
DISPLAY SELECT 1A3S7–A	KA60–1	1A	C
	KA60–2	1A	A
	SLAR	1A	B
	IR	1A	B
	KA76	1A	B
	CDM	1A	B
DISPLAY SELECT 1A3S7–B	KA60–1	1B	F
	KA60–2	1B	D
	SLAR	1B	E
	IR	1B	E
	KA76	1B	E
	CDM	1B	E
MODE SEL 1A3S14	BCD	6B	W
	NUM	6B	X
FRAME NO RESET 1A3S12	DEPRESSED	6B	J
		6B	K
TEST 1A3S13	NOT DEPRESSED	6B	G
	DEPRESSED	6B	V
		Connector 1A3J7 pin:	
TIME SET 1A3S11	NOT DEPRESSED	H	M
	DEPRESSED	H	L
		Front panel test point:	Connector 1A3J6, pin:
DISPLAY SELECT 1A3S7–E	KA60–1	2A	T
	KA60–2	2A	S
	SLAR	2A	R
	IR	2A	R
	KA76	2A	N
	CDM	2A	B
DISPLAY SELECT 1A3S7–C	KA60–1	1C	J
	KA60–2	1C	G
	SLAR	1C	H
	IR	1C	H
	KA76	1C	H
	CDM	1C	H
DISPLAY SELECT 1A3S7–D	KA60–1	1D	M
	KA60–2	1D	K
	SLAR	1D	L
	IR	1D	L
	KA76	1D	L
	CDM	1D	L

Switch	Position	From	To
		Front panel test point:	Connector 1A8J4, pin:
SLAR RANGE 1A8S3	25	5C	C
	50	5C	B
	90	5C	A
SLAR RANGE DELAY 1A8S2	0	5C	K
	10	5C	J
	20	5C	H
	30	5C	G
	40	5C	F
	50	5C	E
	60	5C	D
IR FILTER 1A8S6-B	1	6D	a
	2	6D	b
	3	6D	c
	4	6D	d
	5	6D	e
CYCLING RATE 1A8S1	EXTERNAL	10D	Z
		10D	Y
			Connector 1A8J5, pin:
PRIORITY 1A8S7	KA60-1	6B	x
		18D	v
	KA60-2	6B	v
		18D	x
KA-76 ANGULAR POSITION 1A8S5.	1	6D	GG
	2	6D	FF
	4	6D	EE
	5	6D	DD
		Front panel test point:	Transformer 1A8A5T1, terminal No.:
ROLL 1A8S1-A	−30°	8A	10
	−25°	8A	9
	−20°	8A	8
	−15°	8A	7
	−10°	8A	6
	−5°	8A	5
	0°	8A	3
	5°	8A	3
	10°	8A	3
	15°	8A	3
	20°	8A	3
	25°	8A	3
	30°	8A	3
ROLL 1A8S1-B	−30°	8B	17
	−25°	8B	16
	−20°	8B	15
	−15°	8B	14
	−10°	8B	13
	−5°	8B	12
	0°	8B	11
	5°	8B	12
	10°	8B	13
	15°	8B	14
	20°	8B	15
	25°	8B	16
	30°	8B	17
ROLL 1A8S1-C	−30°	8C	3
	−25°	8C	3
	−20°	8C	3
	−15°	8C	3
	−10°	8C	3
	−5°	8C	3
	0°	8C	4
	5°	8C	5

Switch	Position	From	To
		Front panel test point:	Transformer 1A3A5T1, terminal No.:
	10°	8C	6
	15°	8C	7
	20°	8C	8
	25°	8C	9
	30°	8C	10
			Transformer 1A3A5T2, terminal No.:
PITCH 1A3S4–A	−9°	7C	10
	−7°	7C	9
	−5°	7C	8
	−3°	7C	7
	−2°	7C	6
	−1°	7C	5
	0°	7C	3
	1°	7C	3
	2°	7C	3
	3°	7C	3
	5°	7C	3
	7°	7C	3
	9°	7C	3
PITCH 1A3S4–B	−9°	7D	17
	−7°	7D	16
	−5°	7D	15
	−3°	7D	14
	−2°	7D	13
	−1°	7D	12
	0°	7D	11
	1°	7D	12
	2°	7D	13
	3°	7D	14
	5°	7D	15
	7°	7D	16
	9°	7D	17
PITCH 1A3S4–C	−9°	8D	3
	−7°	8D	3
	−5°	8D	3
	−3°	8D	3
	−2°	8D	3
	−1°	8D	3
	0°	8D	4
	1°	8D	5
	2°	8D	6
	3°	8D	7
	5°	8D	8
	7°	8D	9
	9°	8D	10
			Connector 1A3J4, pin:
IR FILTER S6–A	1	5D	a
	2	5D	b
	3	5D	c
	4	5D	d
	5	5D	e
		Connector 1A3AJ4, pin:	Connector 1A3J4, pin:
CYCLING RATE 1A3S1	EXTERNAL	V	Z
		V	Y
		Connector 1A3A3J, pin:	Front panel test point:
NAVIGATION DATA 10° 1A3S9–A	0	7	6B
	0	6	6B
	1	28	6B
	2	28	6B

Switch	Position	From Connector 1A3A3J1, pin:	To Front panel test point:
	2	7	6B
	3	28	6B
	3	6	6B
	4	28	6B
	4	6	6B
	4	7	6B
	5	29	6B
	6	29	6B
	6	7	6B
	7	29	6B
	7	6	6B
	8	29	6B
	8	6	6B
	8	7	6B
	9	28	6B
	9	29	6B
NAVIGATION DATA 10¹ 1A3S9–B	0	35	6B
	0	36	6B
	1	37	6B
	2	37	6B
	2	36	6B
	3	37	6B
	3	35	6B
	4	36	6B
	4	35	6B
	4	37	6B
	5	5	6B
	6	5	6B
	6	36	6B
	7	5	6B
	7	35	6B
	8	5	6B
	8	35	6B
	8	36	6B
	9	5	6B
	9	37	6B
NAVIGATION DATA 10² 1A3S9–C	0	30	6B
	0	32	6B
	1	33	6B
	2	33	6B
	2	30	6B
	3	32	6B
	3	33	6B
	4	30	6B
	4	32	6B
	4	33	6B
	5	34	6B
	6	34	6B
	6	30	6B
	7	34	6B
	7	32	6B
	8	34	6B
	8	32	6B
	8	30	6B
	9	34	6B
	9	33	6B
NAVIGATION DATA 10³ 1A3S9–D	0	9	6B
	0	10	6B
	1	11	6B
	2	11	6B
	2	9	6B
	3	10	6B

Switch	Position	From	To
		Connector 1A3A2J1, pin:	Front panel test point:
	3	11	6B
	4	9	6B
	4	10	6B
	4	11	6B
	5	15	6B
	6	15	6B
	7	15	6B
	7	10	6B
	8	15	6B
	8	10	6B
	8	9	6B
	9	15	6B
	9	11	6B
NAVIGATION DATA 10' 1A3S9–E	0	10	6B
	0	21	6B
	1	57	6B
	2	57	6B
	2	10	6B
	3	57	6B
	3	21	6B
	4	10	6B
	4	21	6B
	4	57	6B
	5	54	6B
	6	54	6B
	6	10	6B
	7	54	6B
	7	21	6B
	8	54	6B
	8	21	6B
	8	10	6B
	9	54	6B
	9	57	6B
NAVIGATION DATA 10' 1A3S9–F	0	55	6B
	0	58	6B
	1	59	6B
	2	59	6B
	2	55	6B
	3	58	6B
	3	59	6B
	4	55	6B
	4	58	6B
	4	59	6B
	5	60	6B
	6	60	6B
	6	55	6B
	7	60	6B
	7	58	6B
	8	60	6B
	8	58	6B
	8	55	6B
	9	59	6B
	9	60	6B
		Connector 1A3A2J1, pin:	Connector 1A3J3, pin:
FOCAL LENGTH (units) 1A3S8–C	0	29	X
	0	33	X
	1	21	X
	2	29	X
	2	21	X
	3	33	X
	3	21	X

Switch	Position	From	To
		Connector 1A8A2J1, pin:	Connector 1A8J8, pin:
	4	29	X
	4	33	X
	4	21	X
	5	26	X
	6	29	X
	6	26	X
	7	33	X
	7	26	X
	8	26	X
	8	33	X
	8	29	X
	9	21	X
	9	26	X
FOCAL LENGTH (tens) 1A8S6-D	0	30	s
	0	32	s
	1	22	s
	2	22	s
	2	30	s
	3	22	s
	3	32	s
	4	22	s
	4	32	s
	4	30	s
	5	28	s
	6	28	s
	6	30	s
	7	28	s
	7	32	s
	8	28	s
	8	32	s
	8	30	s
	9	22	s
	9	28	s
		Connector 1A8J8, pin:	Connector 1A8J7, pin:
TIME (units) 1A8S8-A	0	f	L
	0	g	L
	1	i	L
	2	i	L
	2	f	L
	3	i	L
	3	g	L
	4	i	L
	4	g	L
	4	f	L
	5	j	L
	6	j	L
	6	f	L
	7	j	L
	7	g	L
	8	j	L
	8	g	L
	8	f	L
	9	j	L
	9	i	L
TIME (tens) 1A8S8-B	0	a	L
	0	Z	L
	1	e	L
	2	e	L
	2	Z	L
	3	e	L
	3	a	L
	4	e	L

Switch	Position	From	To
		Connector 1A3J8, pin:	Connector 1A3J7, pin:
	4	a	L
	4	Z	L
	5	d	L
	6	d	L
	6	Z	L
	7	d	L
	7	a	L
	8	d	L
	8	a	L
	8	Z	L
	9	d	L
	9	c	L
		Connector 1A3J7, pin:	Connector 1A3J8, pin:
EXPSR 1A3S10-A	1	H	P
	2	H	n
	3	H	n
	3	H	p
	4	H	m
	5	H	p
	5	H	m
	6	H	m
	6	H	n
	7	H	m
	7	H	n
	7	H	p
		Connector 1A3J8, pin:	Connector 1A3J8, pin:
DAY (tens) 1A3S10-G	0	B	R
	1	C	R
	2	D	R
	3	E	R
DAY (units) 1A3S10-F	0	B	S
	1	C	S
	2	D	S
	3	E	S
	4	F	S
	5	G	S
	6	H	S
	7	J	S
	8	K	S
	9	L	S
MONTH (tens) 1A3S10-E	0	B	T
	1	C	T
MONTH (units) 1A3S10-D	0	B	U
	1	C	U
	2	D	U
	3	E	U
	4	F	U
	5	G	U
	6	H	U
	7	J	U
	8	K	U
	9	L	U
YEAR (tens) 1A3S10-C	0	V	V
	1	C	V
	2	D	V
	3	E	V
	4	F	V
	5	G	V
	6	H	V
	7	J	V
	8	K	V
	9	L	V

Switch	Position	From Connector 1A3J8, pin:	To Connector 1A3J8, pin:
YEAR (units) 1A3S10–B	0	B	W
	1	C	W
	2	D	W
	3	E	W
	4	F	W
	5	G	W
	6	H	W
	7	J	W
	8	K	W
	9	L	W
SORTIE AND TAKING UNIT (Units) 1A3S8–E.	0	B	P
	1	C	P
	2	D	P
	3	E	P
	4	F	P
	5	G	P
	6	H	P
	7	J	P
	8	K	P
	9	L	P
SORTIE AND TAKING UNIT (Tens) 1A3S8–F.	0	B	N
	1	C	N
	2	D	N
	3	E	N
	4	F	N
	5	G	N
	6	H	N
	7	J	N
	8	K	N
	9	L	N
SORTIE TAKING UNIT (Hundreds) 1A3S8–G.	0	B	M
	1	C	M
	2	D	M
	3	E	M
	4	F	M
	5	G	M
	6	H	M
	7	J	M
	8	K	M
	9	L	M

3-9. Test Points Location

Front panel test points on the SDC test set are illustrated and presented in figure 3–2 and table 3–6 respectively. The *TP* column refers to front panel test points. The *Signal* column refers to signal normally present at that test point.

3-10. Parts Location

Locate all parts on figure which support the removal and replacement procedures (para 3–12).

Table 3-6. Front Panel Test Points

TP	Signal
1A	VD (vertical deflection)
1B	−HD (horizontal deflection)
1C	+HD (horizontal deflection)
1D	−VD (vertical deflection)
2A	UNBLANKING SIGNAL
2B	−552 VDC
2C	−442 VDC
2D	+500 VDC
3A	Not used
3B	Not used
3C	Not used
3D	Not used
4A	Not used
4B	Not used
4C	Not used
4D	Not used
5A	26 VAC, 400 Hz
5B	26 VAC RET
5C	+28 VDC
5D	28 VDC RET
6A	+5 VDC
6B	+5 VDC RETURN
6C	DATA READY
6D	SIGNAL GROUND
7A	OUT OF RANGE Vg/H
7B	Not used
7C	PITCH
7D	PITCH
8A	ROLL
8B	ROLL
8C	ROLL
8D	PITCH
9A	IR DATA DEMAND
9B	SLAR DATA DEMAND
9C	KA60 DATA DEMAND
9D	KA76 DATA DEMAND
10A	GROUND (BARO ALT, low side)
10B	BAROMETRIC ALTITUDE (rotor arm)
10C	BAROMETRIC ALTITUDE (reference)
10D	(WIPER OF R3) Vg/H to KA60's
11A	AL–1
11B	AL–2
11C	AL–3
11D	+140 VDC
12A	INS1
12B	INS2
12C	INS3
12D	INS4
13A	INS5
13B	INS6
13C	INS7
13D	INS8
14A	INS9
14B	INS10
14C	INS11
14D	INS12
15A	INS13
15B	INS14
15C	INS15
15D	INS16
16A	INS17
16B	INS18
16C	INS19
16D	INS20
17A	INS21
17B	INS22
17C	INS23
17D	INS24
18A	SIG GND
18B	+5 VDC (GO/NO GO)
18C	Not used
18D	KA60 DATA DEMAND

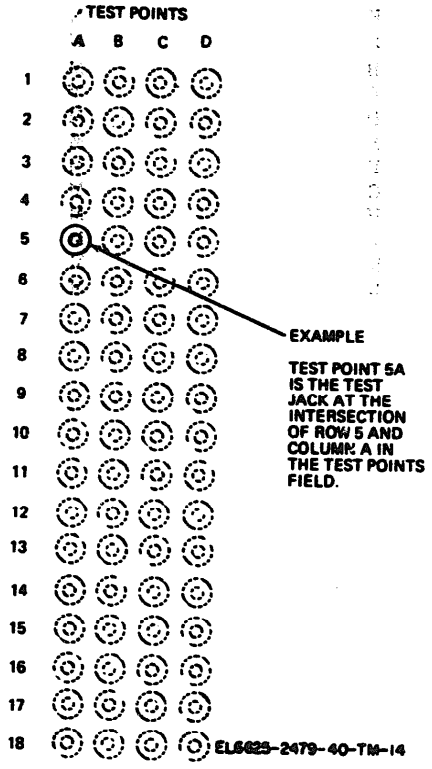

Figure 3-2. Front panel test points.

3-11. System wiring and Interconnection

System wiring and interconnection information is given for the test set in figures 8–3 through 8–7 and figures FO–10 through FO–17. These diagrams show complete point-to-point wiring of the test set and include specific wiring details such as wire and gauge numbers and to—from information.

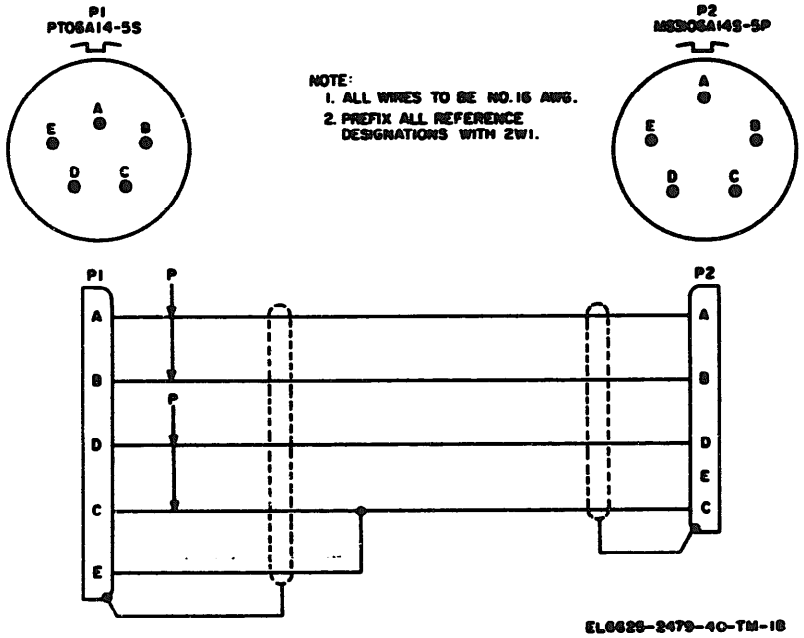

Figure 3-3. Cable Assembly, Power, Electrical CX-12714/AYH-3, wiring diagram.

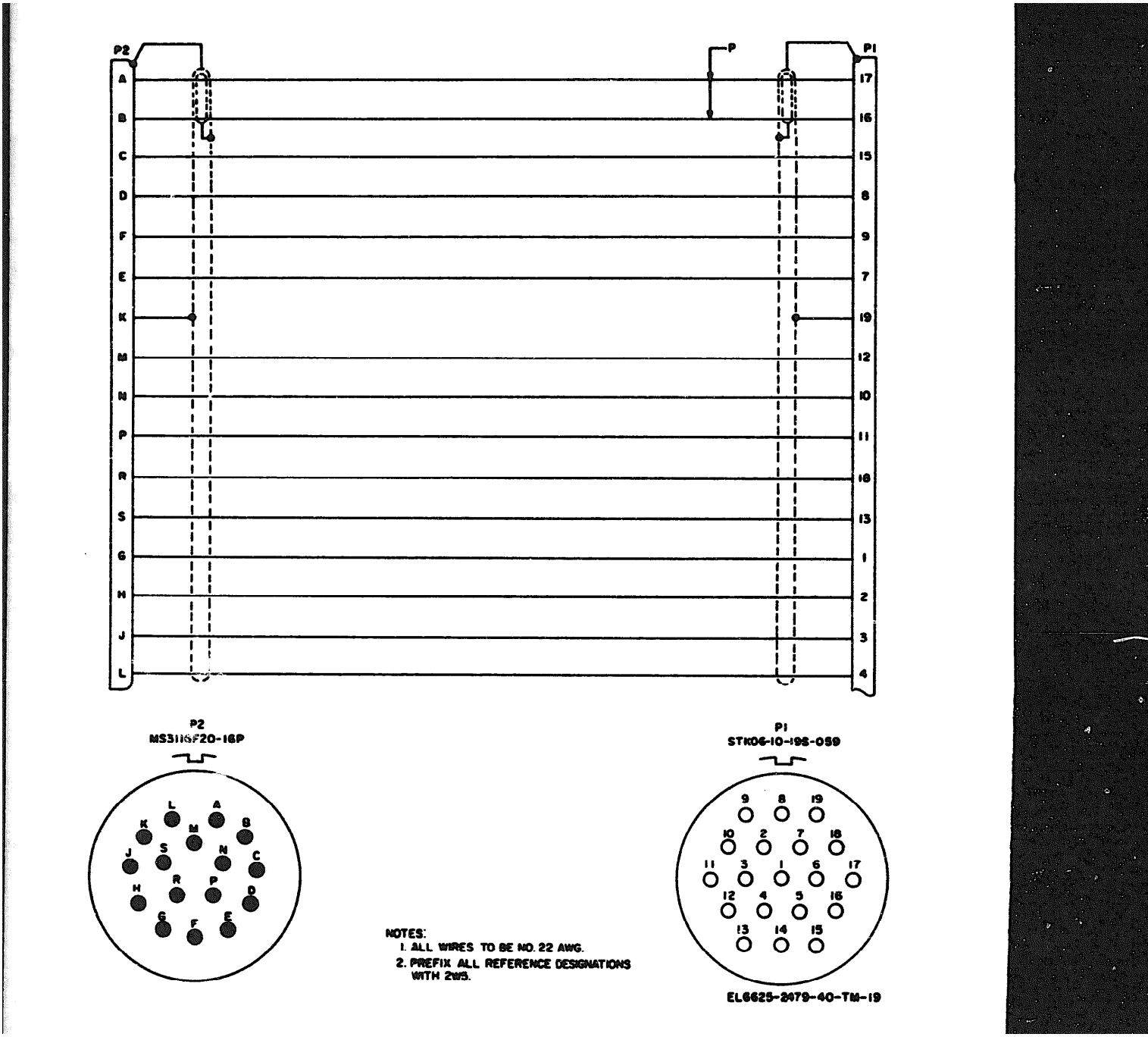

Figure 3-4. Cable Assembly, Special Purpose, Electrical CS-13718/AYM-8. wiring diagram.

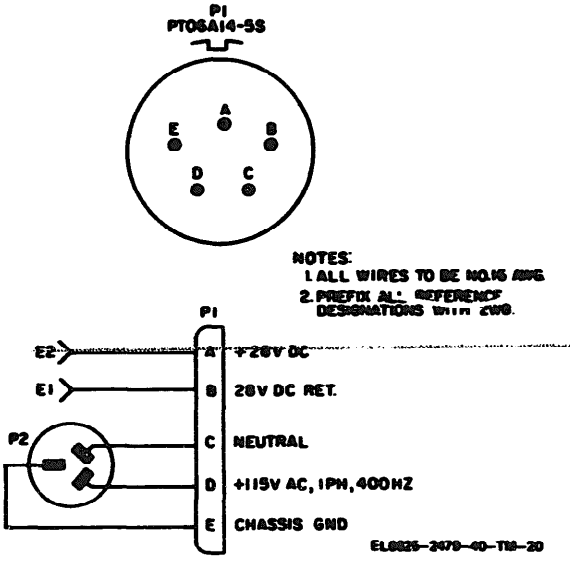

Figure 3-5. Cable Assembly, Power, Electrical, Branched CX-12724/AYM-8, wiring diagram.

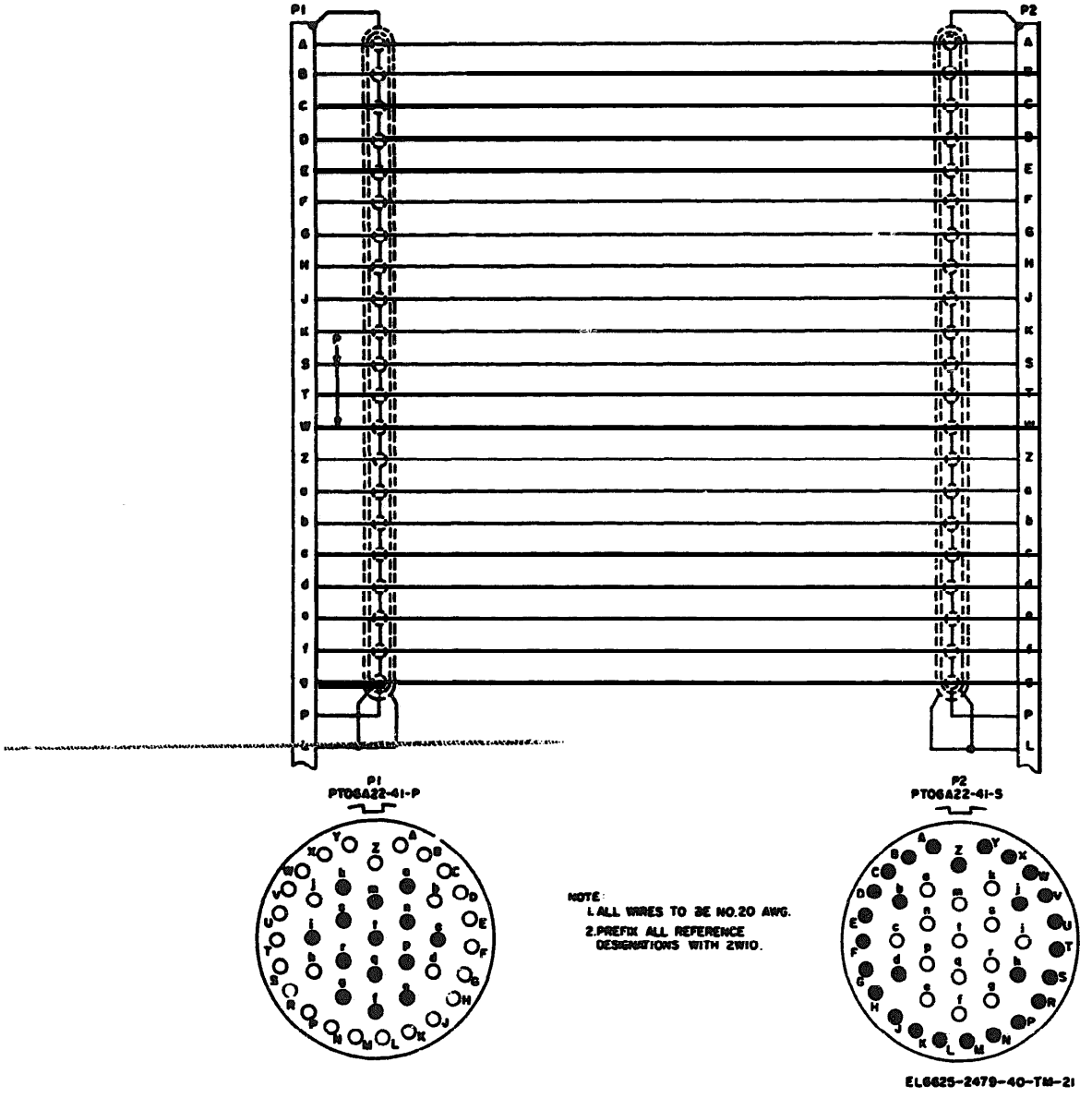

Figure 3-6. Cable Assembly, Special Purpose, Electric CX-12722/AYM-3, wiring diagram

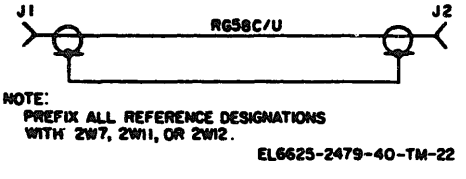

Figure 3-7. Cable Assembly, Radio Frequency CG-3679/SYM-3, wiring diagram.

Section III. REMOVAL AND REPLACEMENT

3-12. Removal

All parts of the test set may be removed using standard tools and maintenance procedures. Refer to parts location illustrations, figures 3-8 through 3-35 when removing parts and subassemblies. The panel assembly (1A3) of Test Set, Signal Data Converter TS-3089/AYM-8 is removed by disengaging the 14 screws along the edge of the panel assembly and lifting the panel assembly from the case (fig. 3-8).

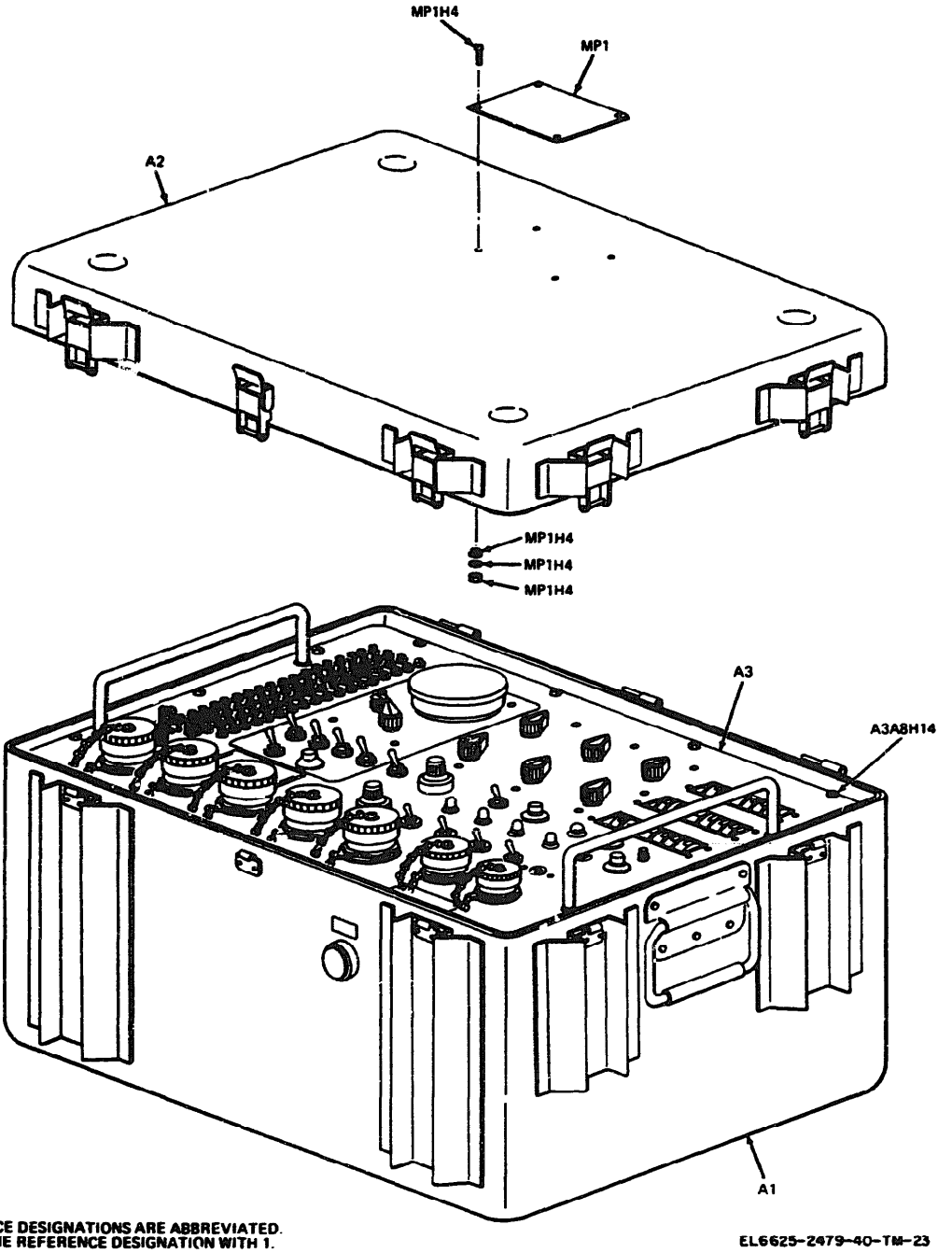

Figure 3-8. Test Set, Signal Data Converter TS-4089/AYM-8, parts location.

3-13. Replacement

All parts may be replaced using standard tools and maintenance procedures. Refer to the parts location illustrations, figures 3–8 through 3–35, when replacing parts and subassemblies. The panel assembly (1A8) of Test Set, Signal Data Converter TS–3089/AYM–8 is replaced by inserting the panel assembly into the case and securing the 14 screws along the edge of the panel assembly to the case (fig. 3–8).

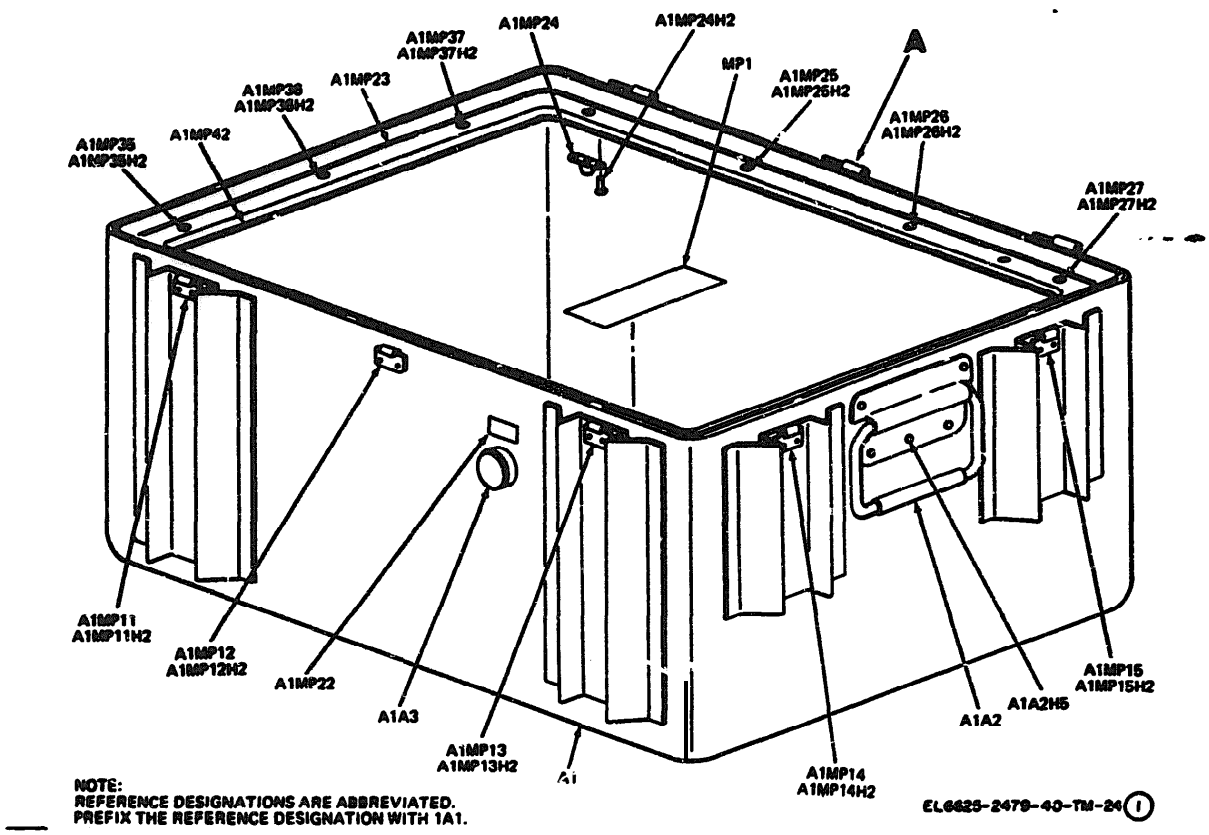

Figure 3-9(1). Case assembly 1A1, parts location (part 1 of 2).

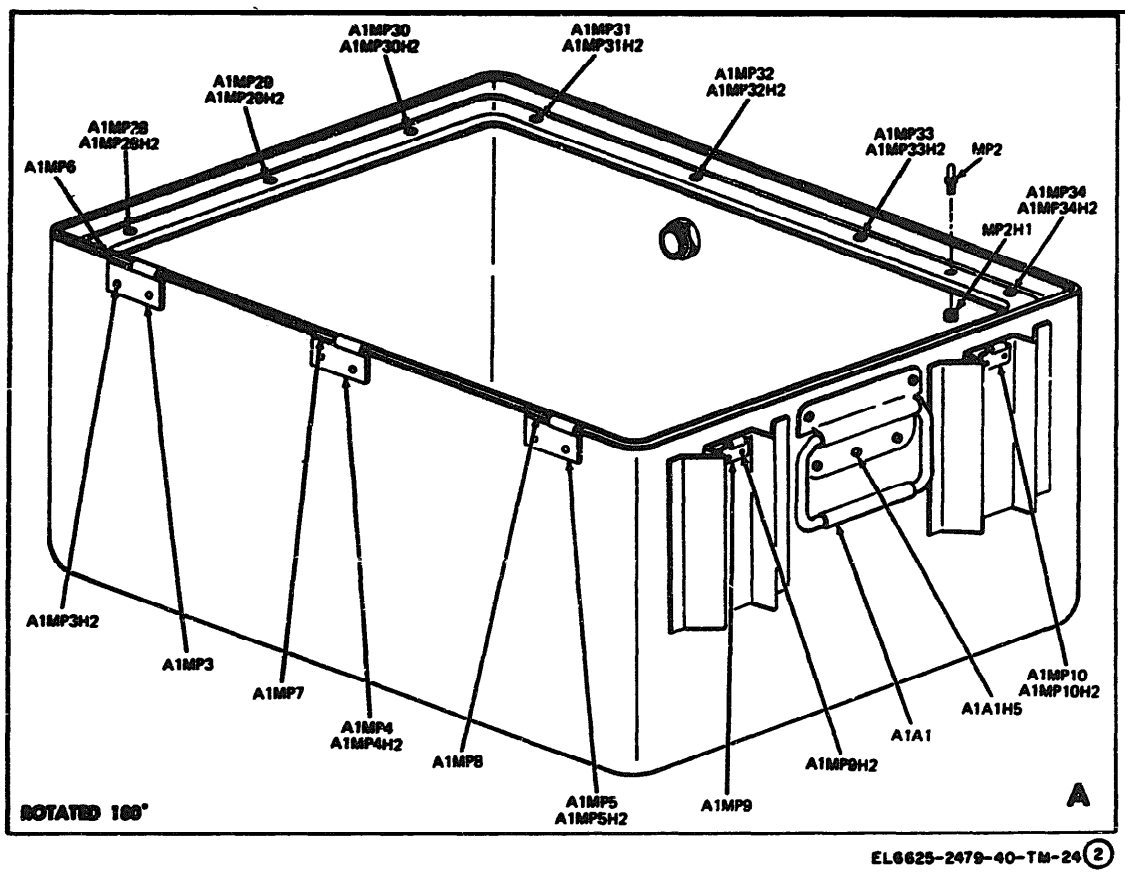

Figure 3-9 (2). Case assembly 1A1, parts location (part 2 of 2).

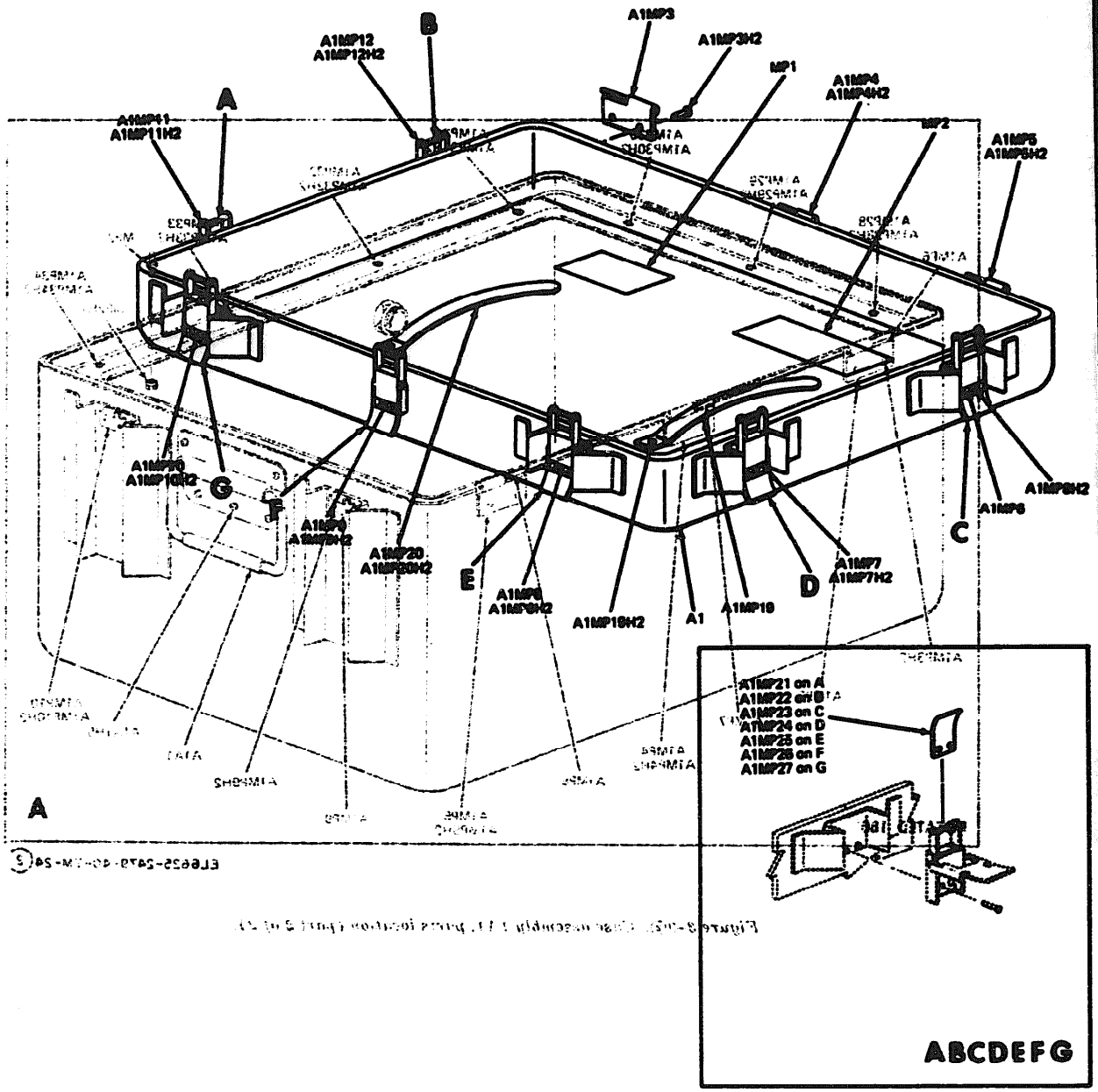

Figure 3-10. Cover, Test Set CW-1348/AYM-3, parts location.

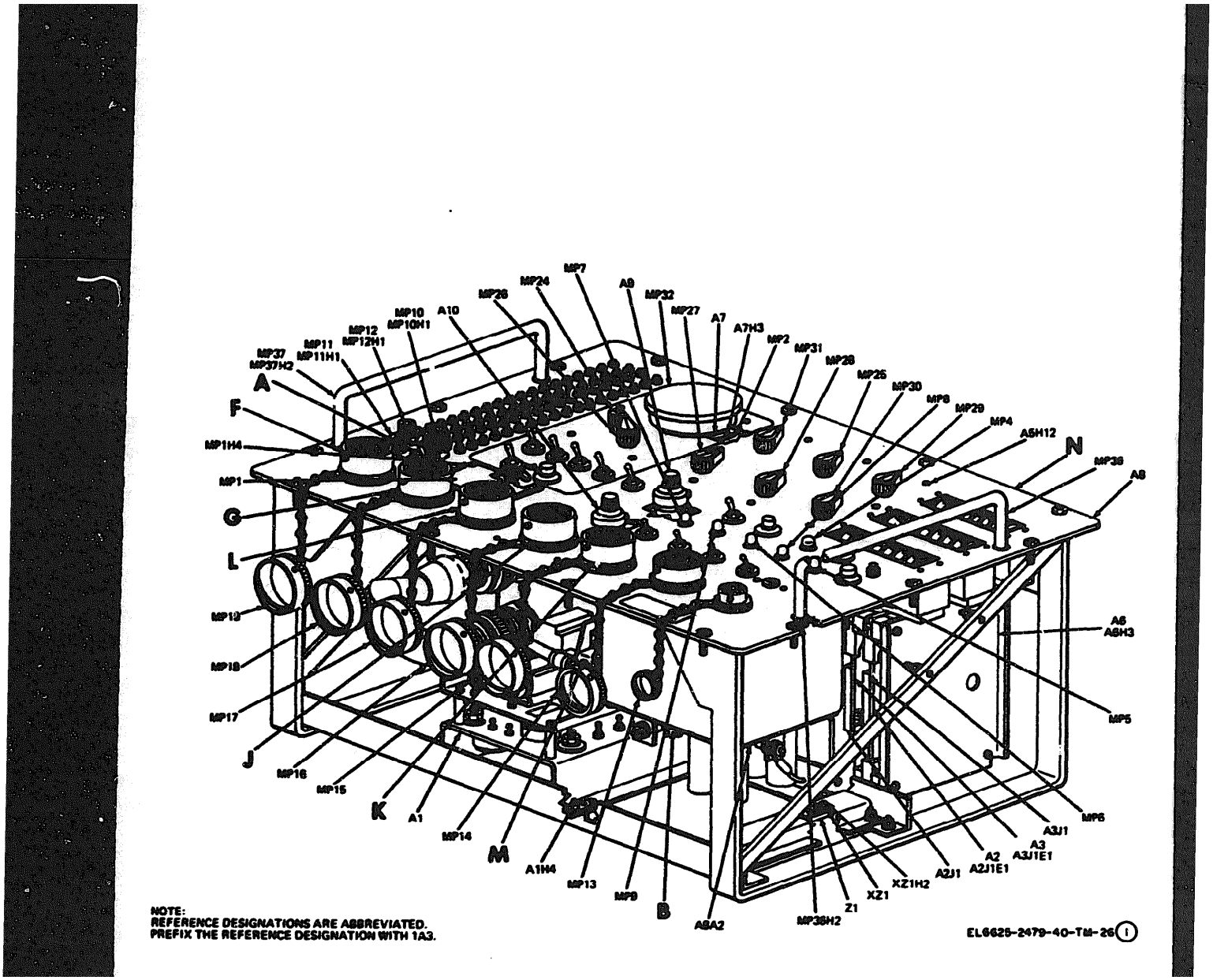

Figure 3-11. Panel assembly 1A3, parts location (part 1 of 5).

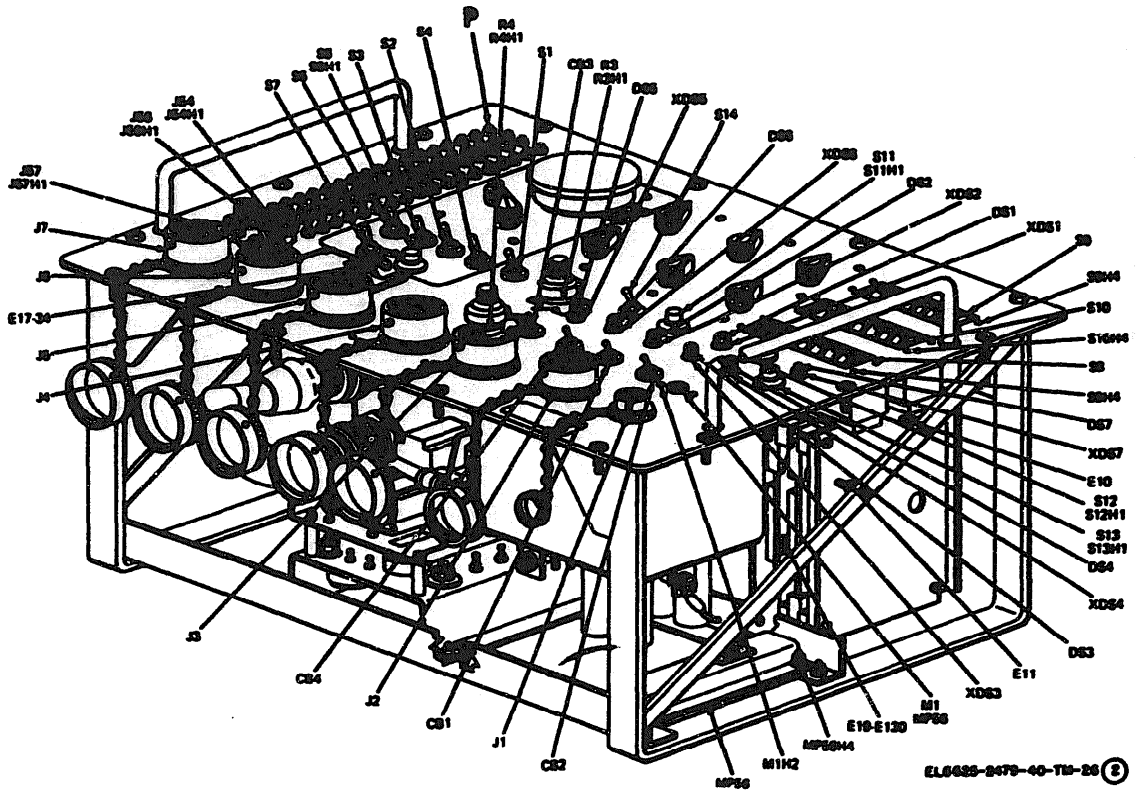

Figure 3-11. Panel assembly 1A3, parts location (part 2 of 5).

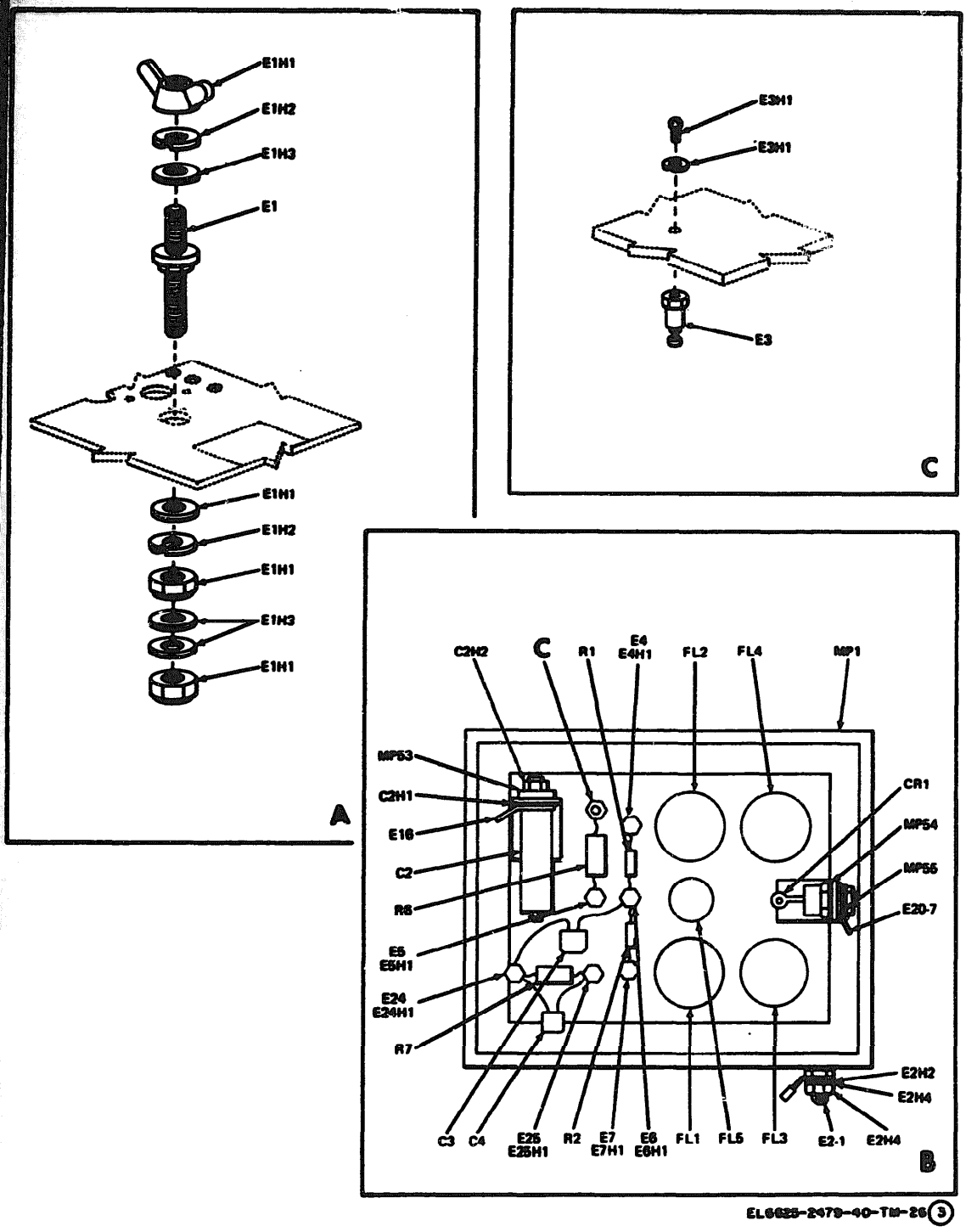

Figure 3-11 D. Panel assembly 1A3, parts location (part 3 of 5).

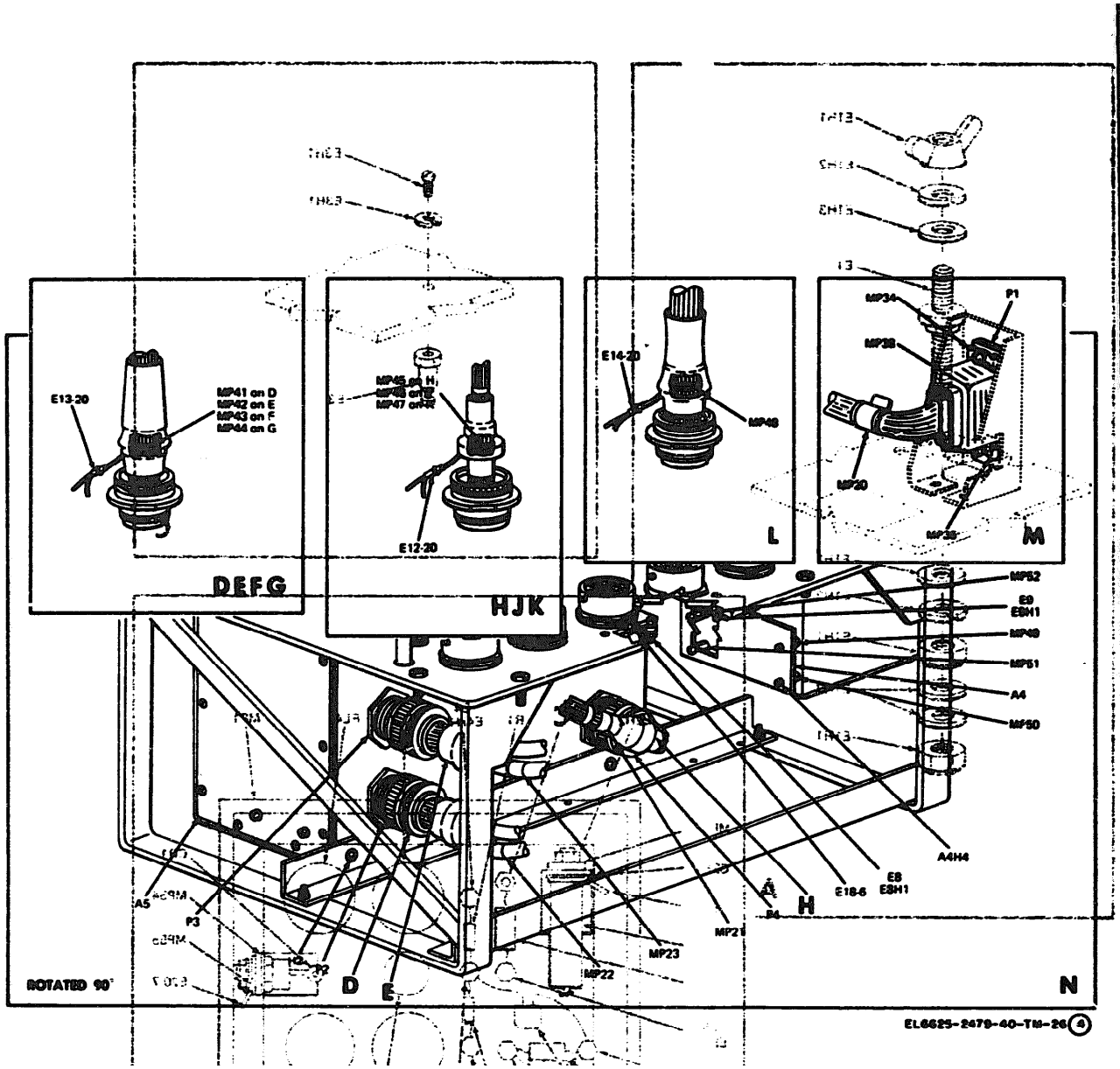

Figure 3-11. Panel assembly 1A3, parts location (parts 4 of 5).

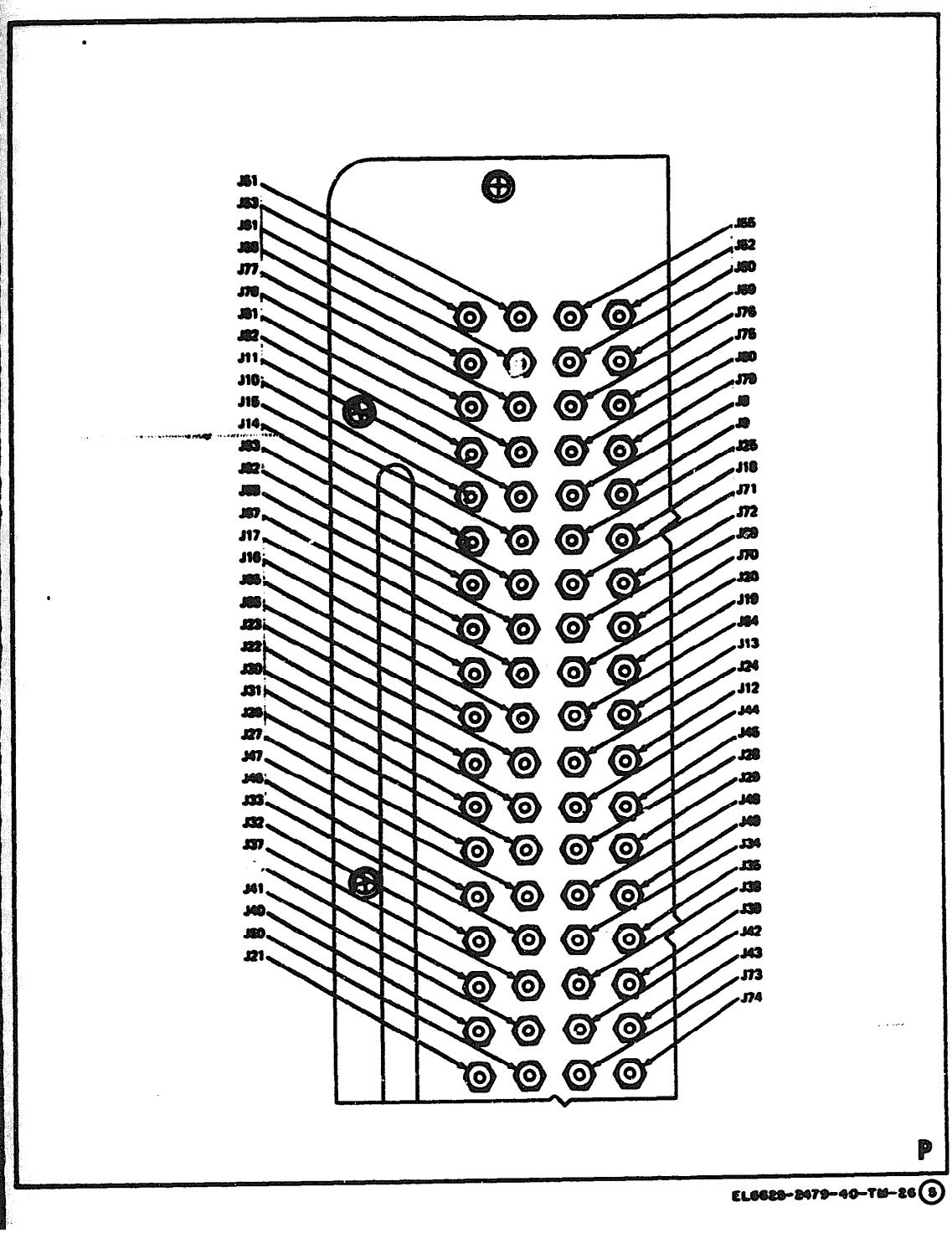

Figure 3-11 (5). Panel assembly 1A3, parts location (part 5 of 5).

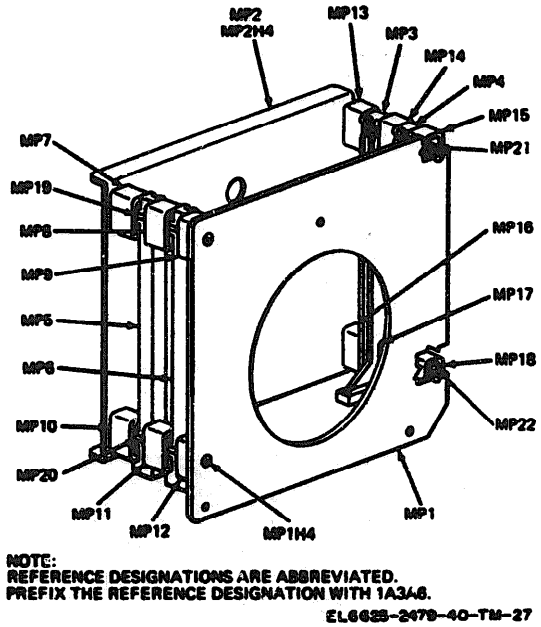

Figure 3-12. Basket assembly 1A3A6, pars location.

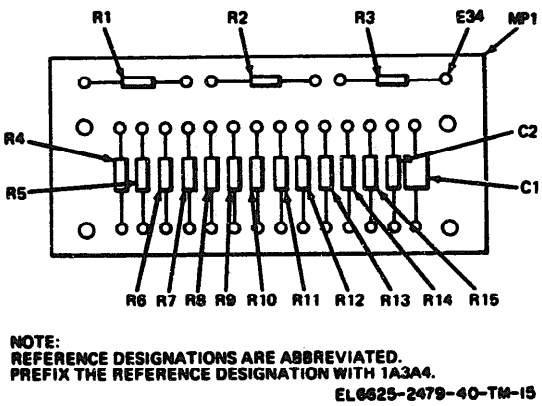

Figure 3-13. Component board assembly 1A3A4, parts location.

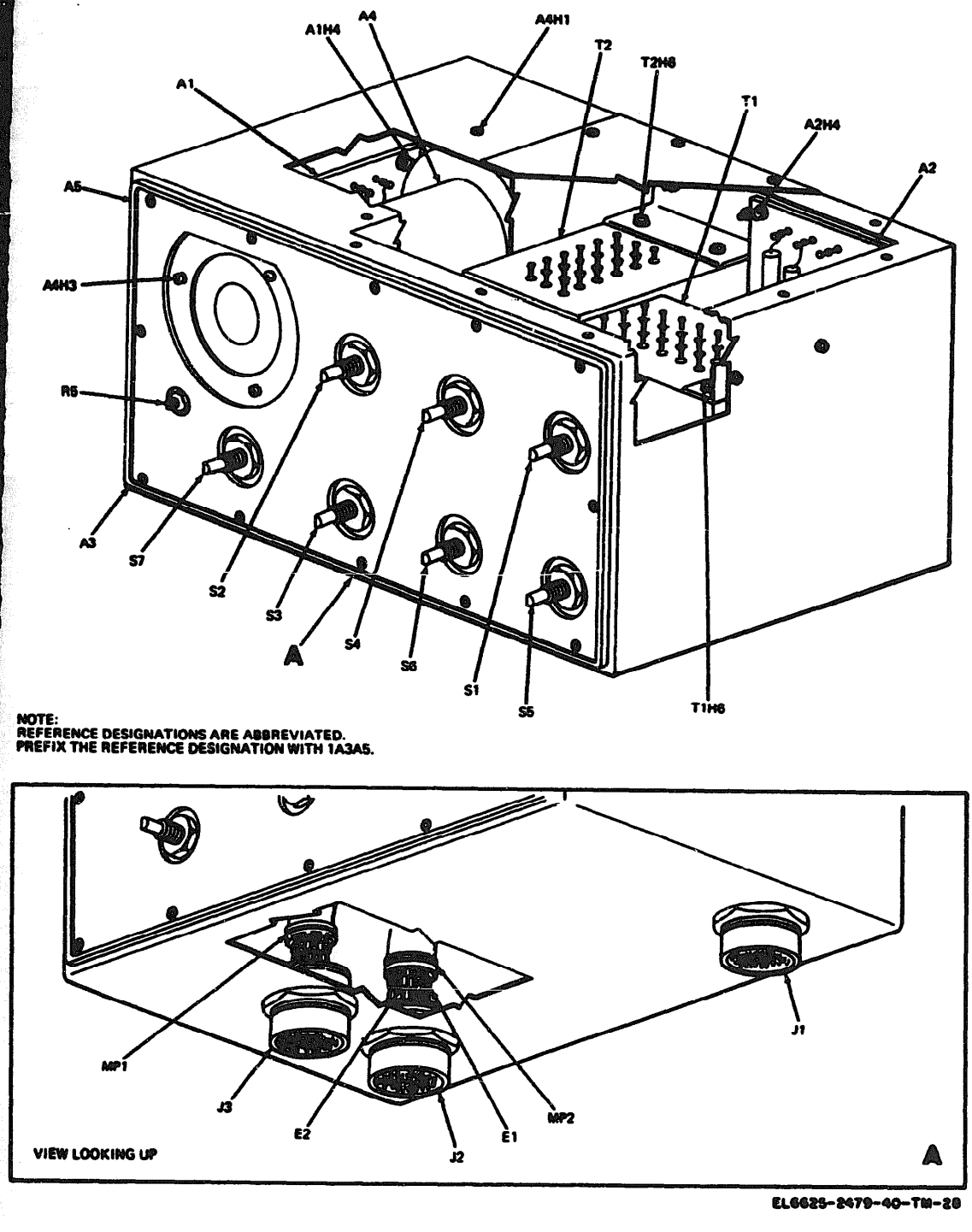

Figure 3-14. Monitor assembly 1A3A5, parts location.

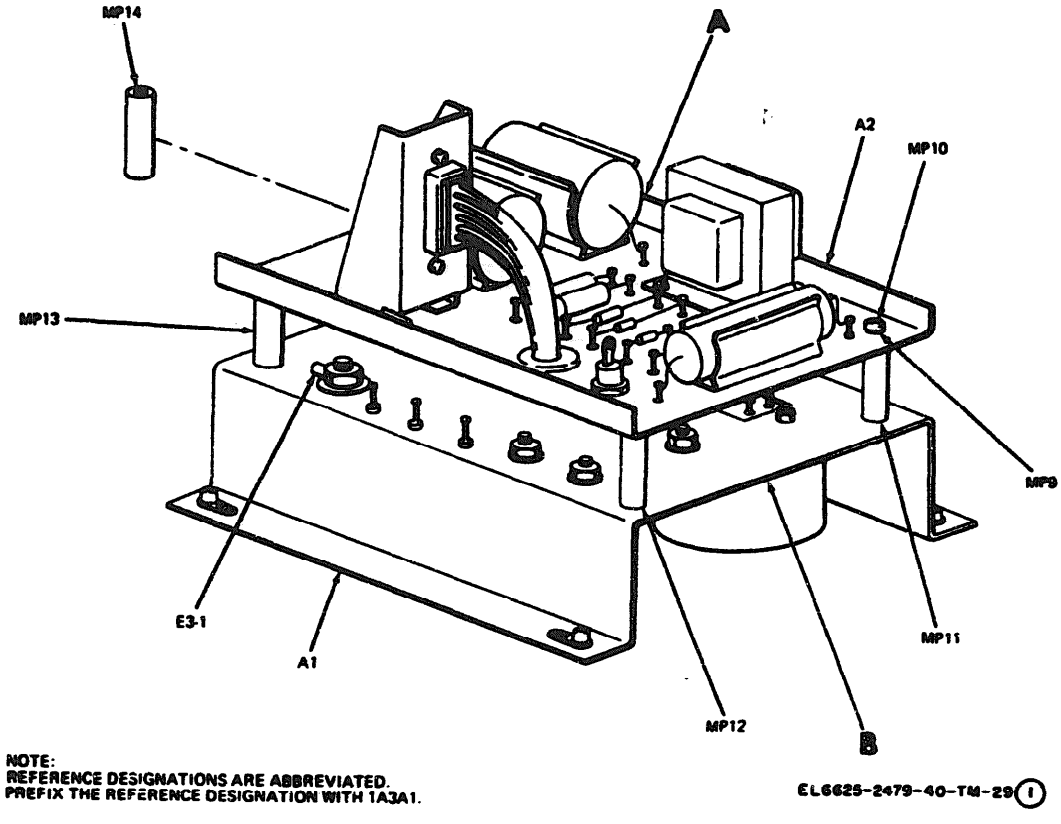

Figure 3-15. (1) Power supply 1A3A1, parts location (part 1 of 3).

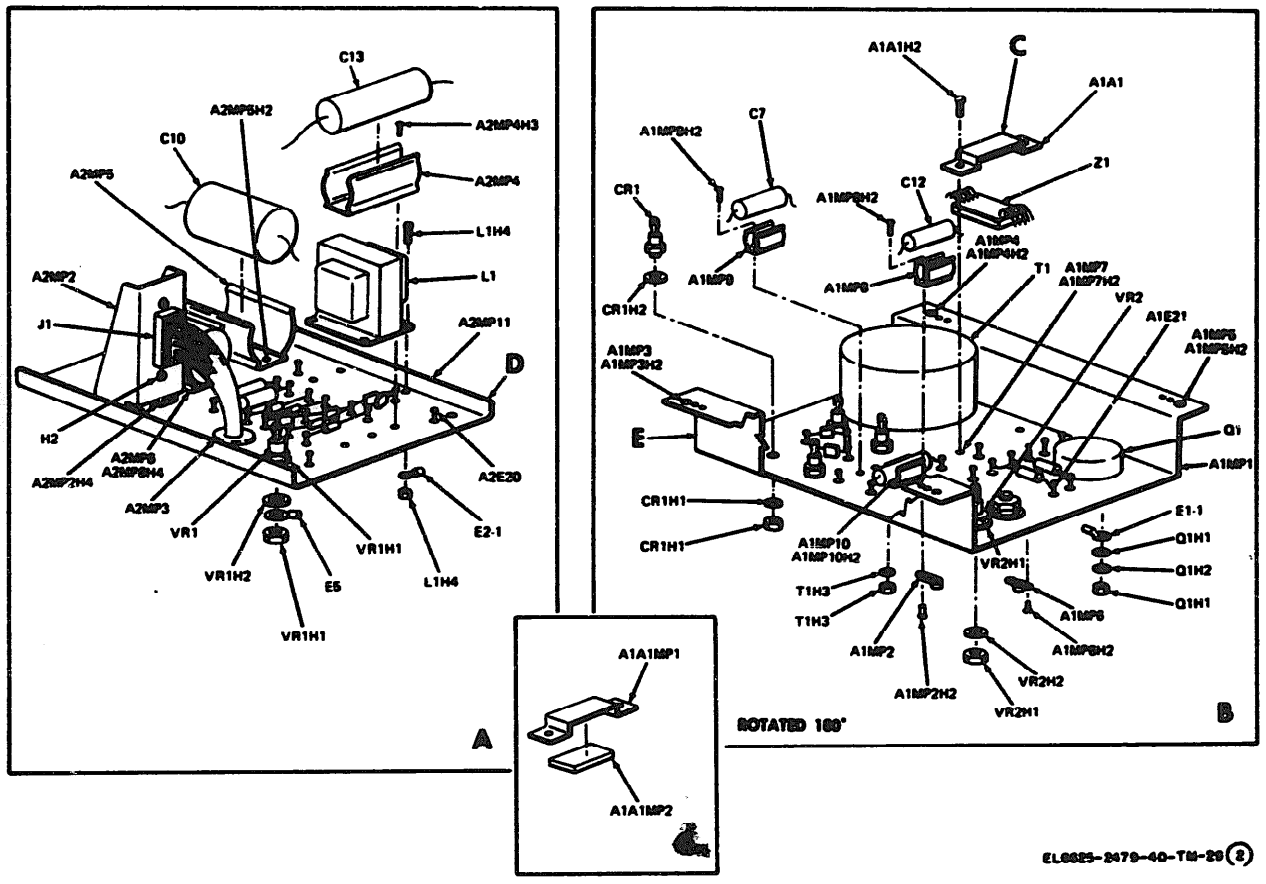

Figure 3-15 (5). Power supply 1A3A1, parts location (part 2 of 2).

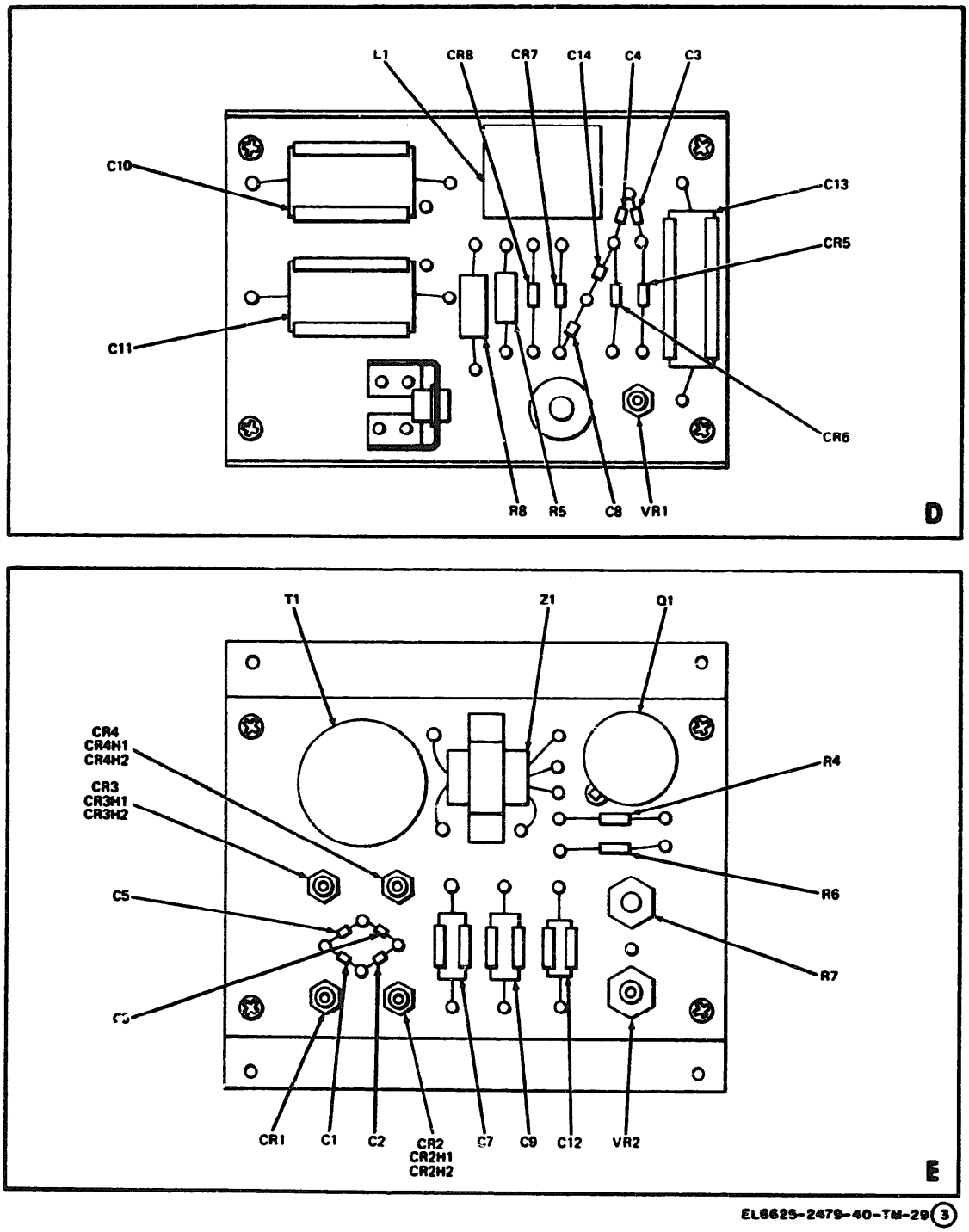

Figure 3-15. Power supply 1A3A1, parts location (part 3 of 3).

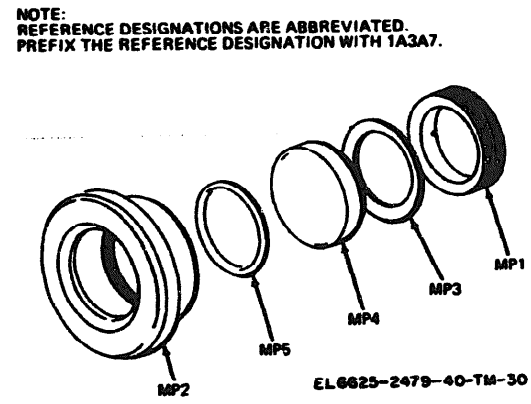

Figure 3-16. Bezel assembly 1A3A7, parts location.

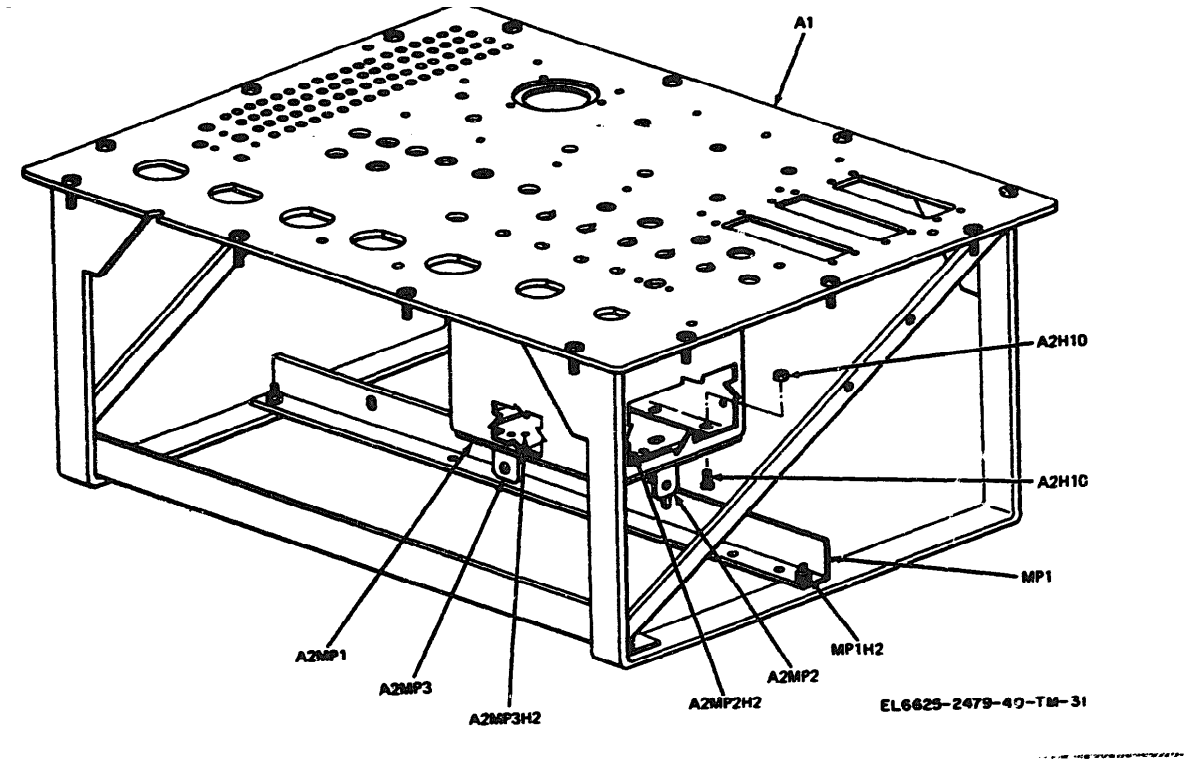

Figure 3-17. Pane and chassis assembly 1A3A8, parts location.

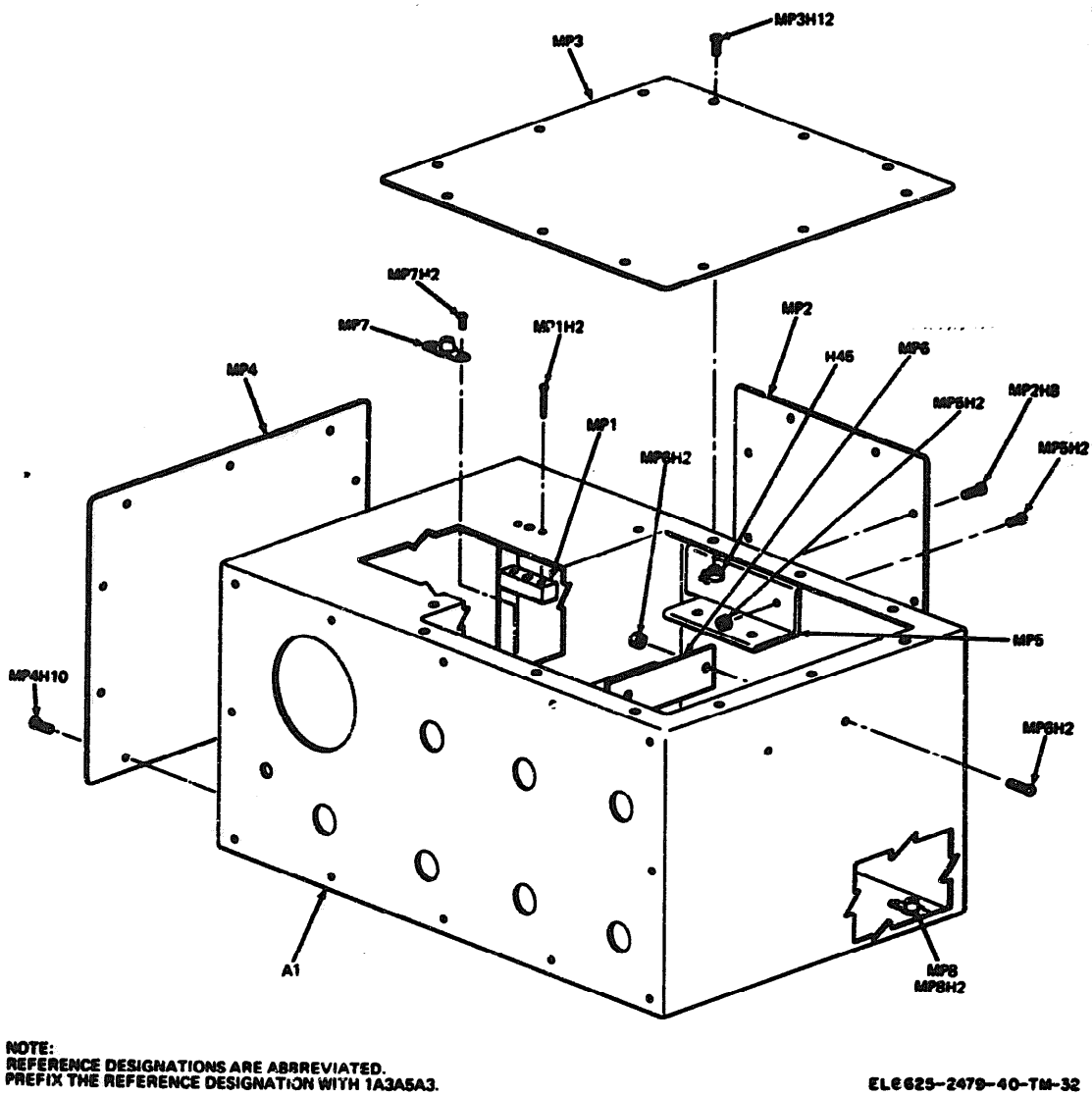

Figure 3-18. Monitor box assembly 1A3A5A3, parts location.

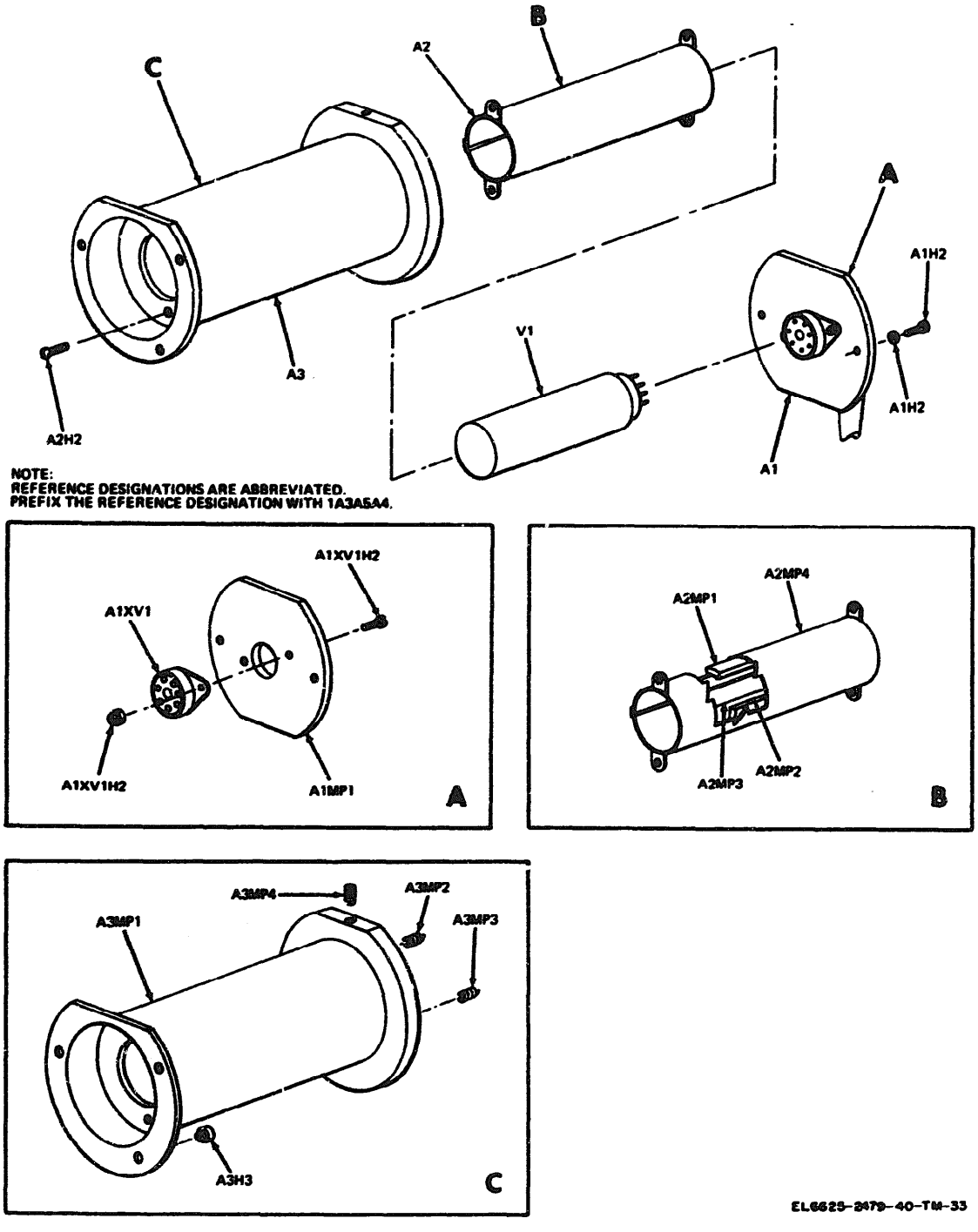

Figure 3-19. Tube housing assembly 1A3A5A4, parts location.

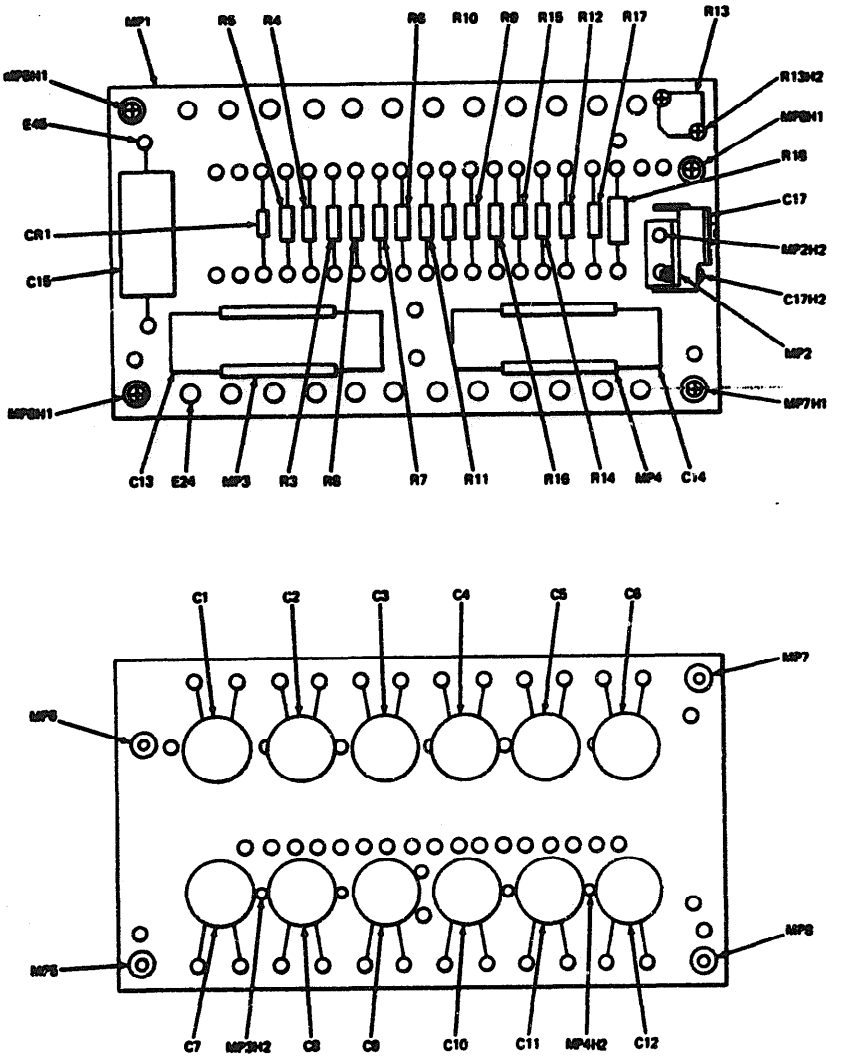

Figure 3-20. Component board assembly 1A3A5A1, parts location.

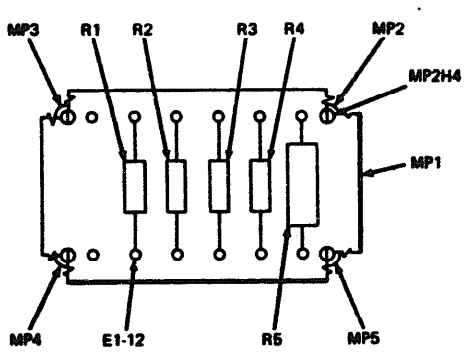

Figure 3-21. Component board assembly 1A3A5A2, parts location.

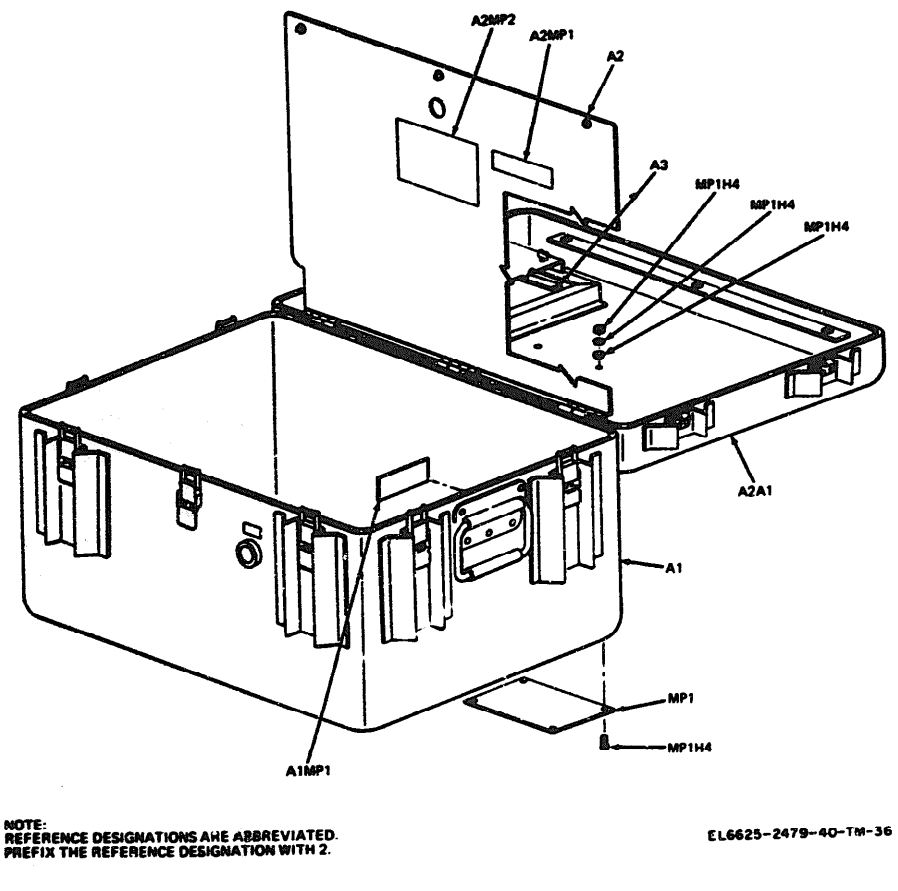

Figure 3-22. Case, Test Set CY-7114/AYM-8, parts location.

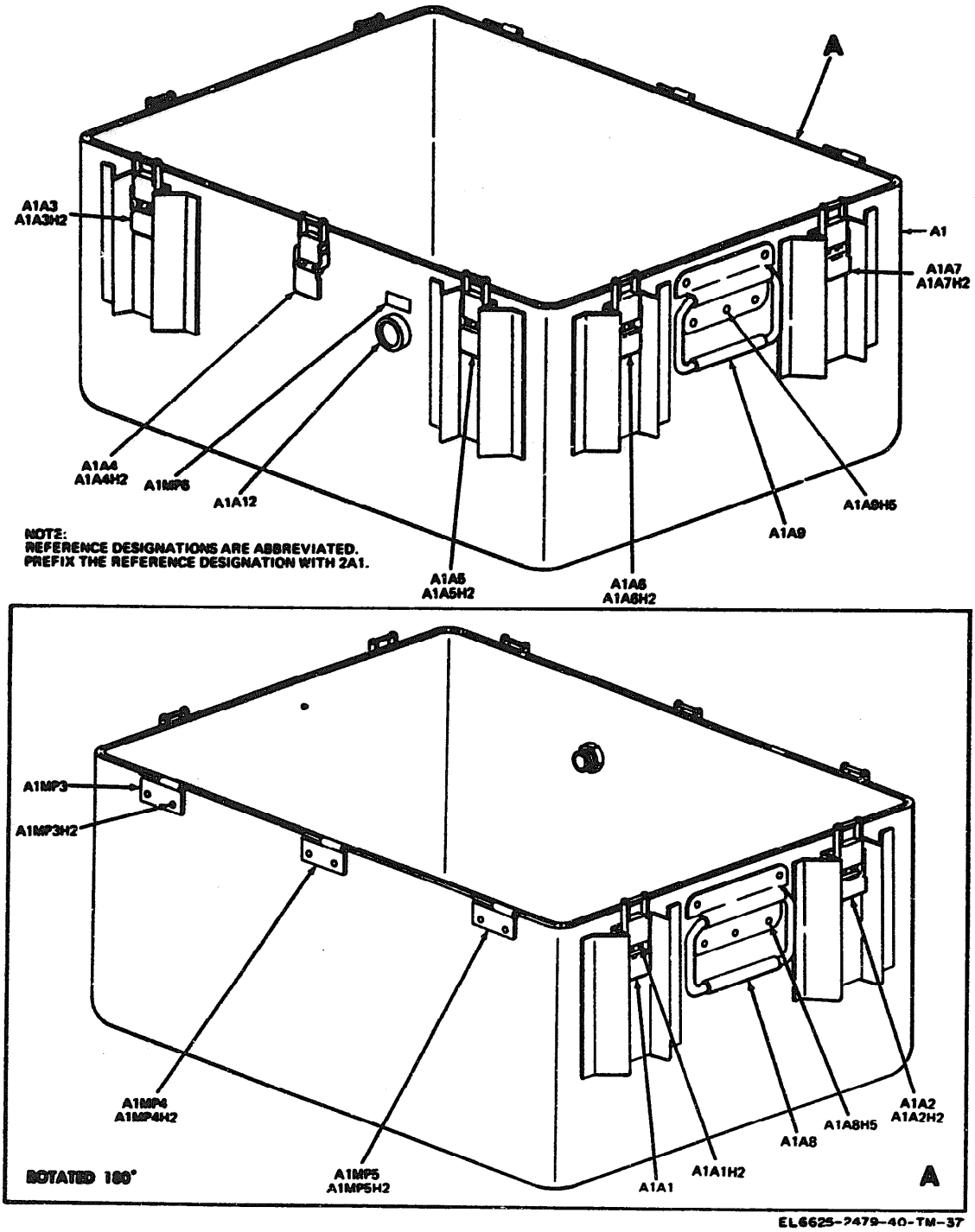

Figure 3-23. Case base assembly 2A1, parts location.

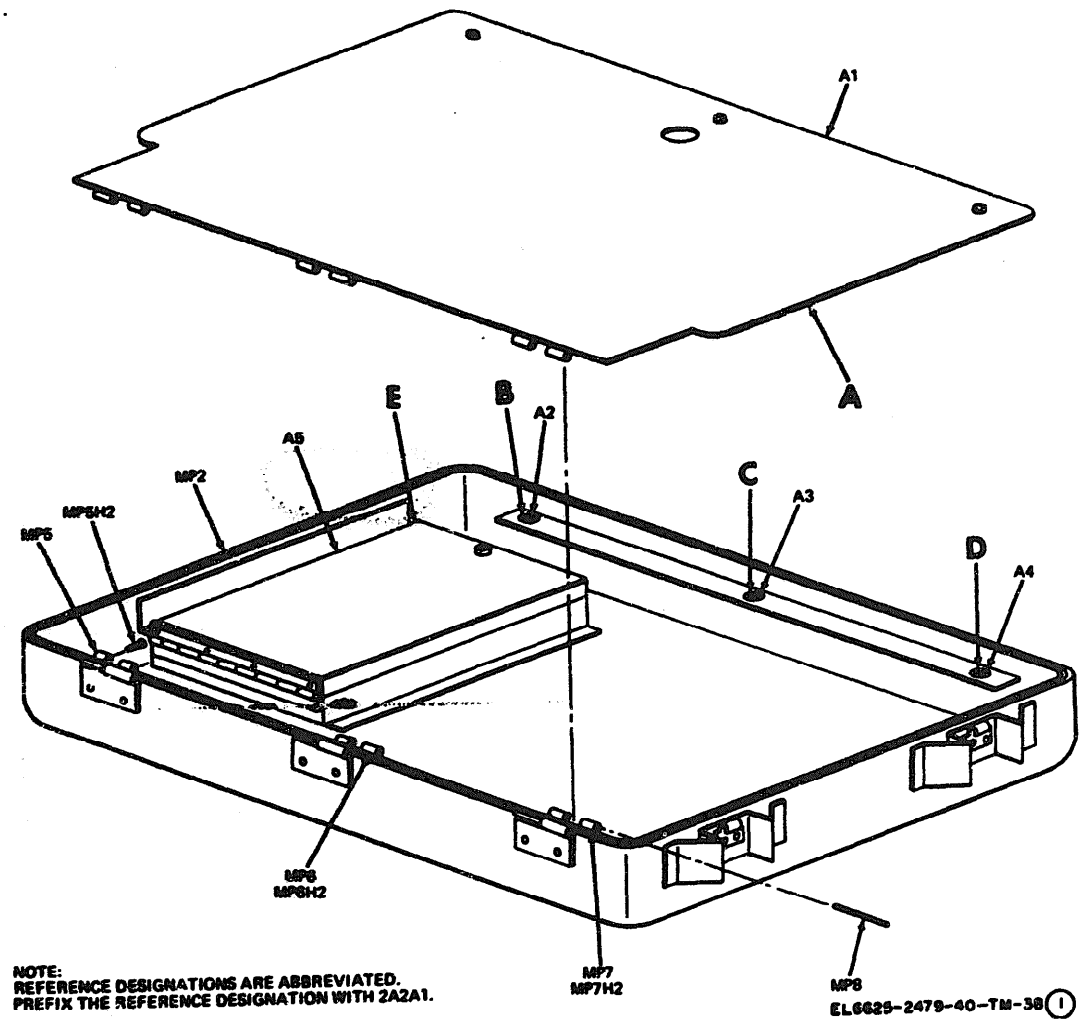

Figure 3-24 (1). Case cover assembly 2S2, parts location (part 1 of 2.)

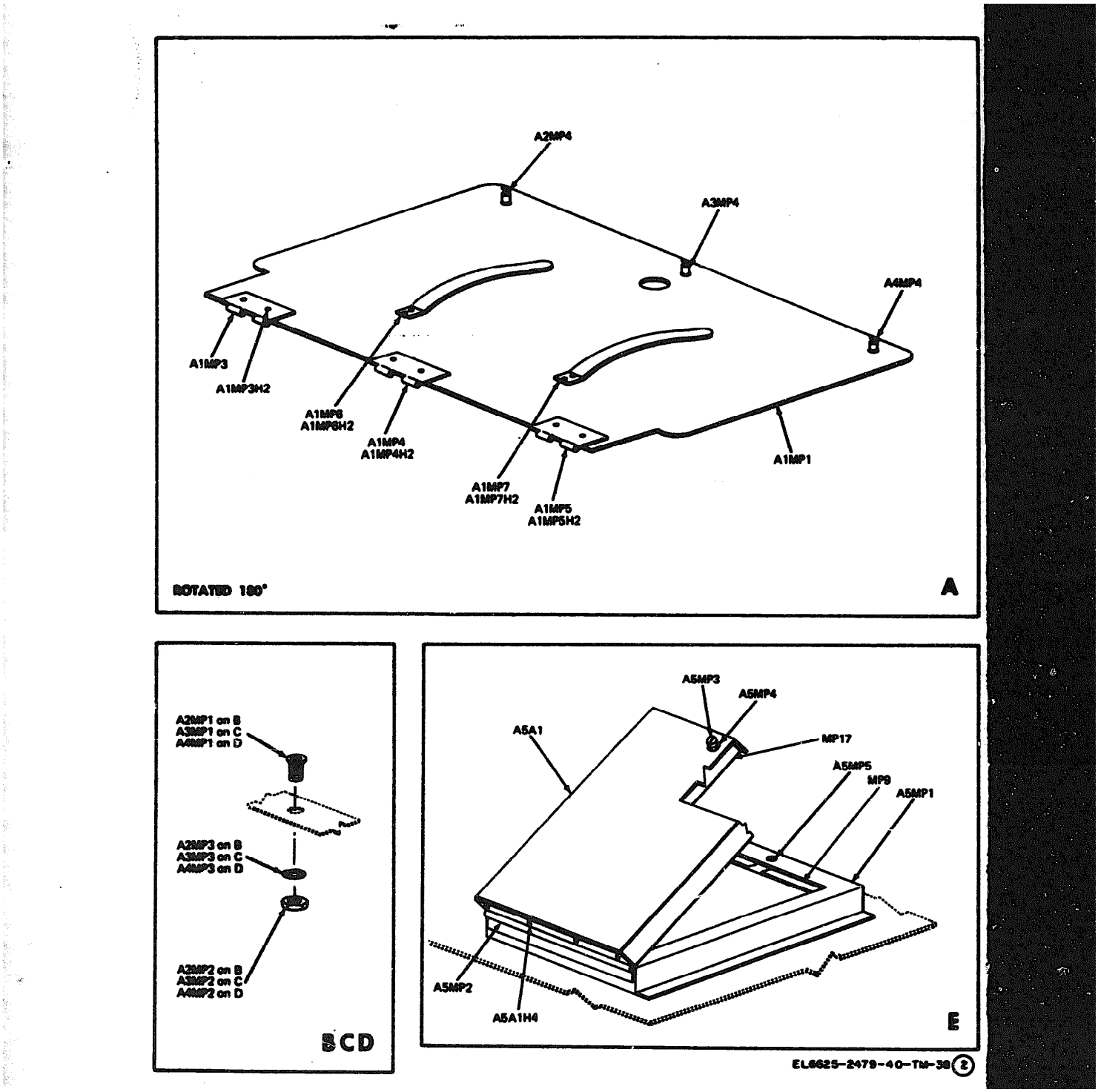

Figure 3-24 (8). Case cover assembly 2A2, parts location (part 2 of 2).

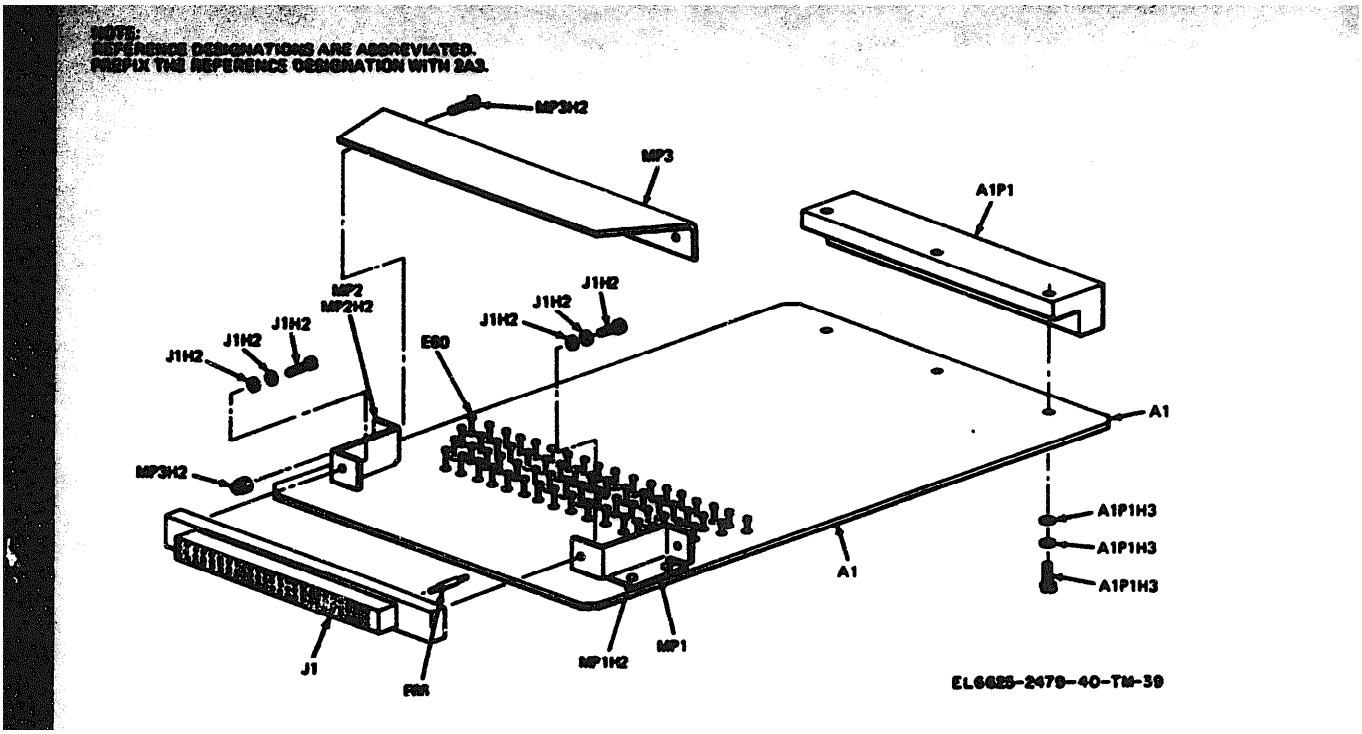

Figure 3-25. Extender, Circuit Card MX-3966/AYM, parts location.

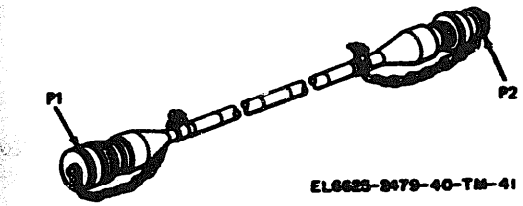

Figure 3-26. Cable Assembly, Special Purpose, Electrical CX-12718/AYM-8, parts location.

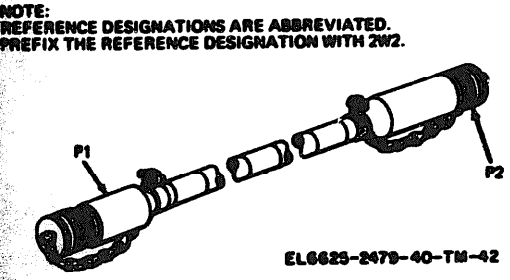

Figure 3-27. Cable Assembly, Special Purpose, Electrical CX-12715/AYM-8, parts location.

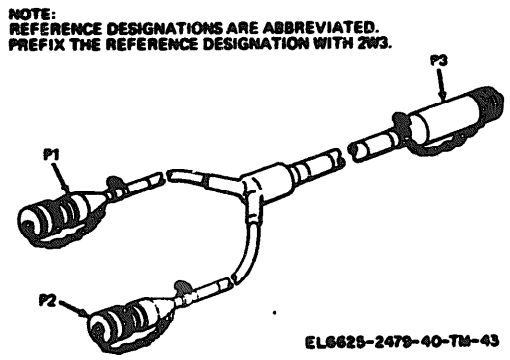

Figure 3-28. Cable Assembly, Special Purpose, Electrical, Branched CX-12716/AYM-8, parts location.

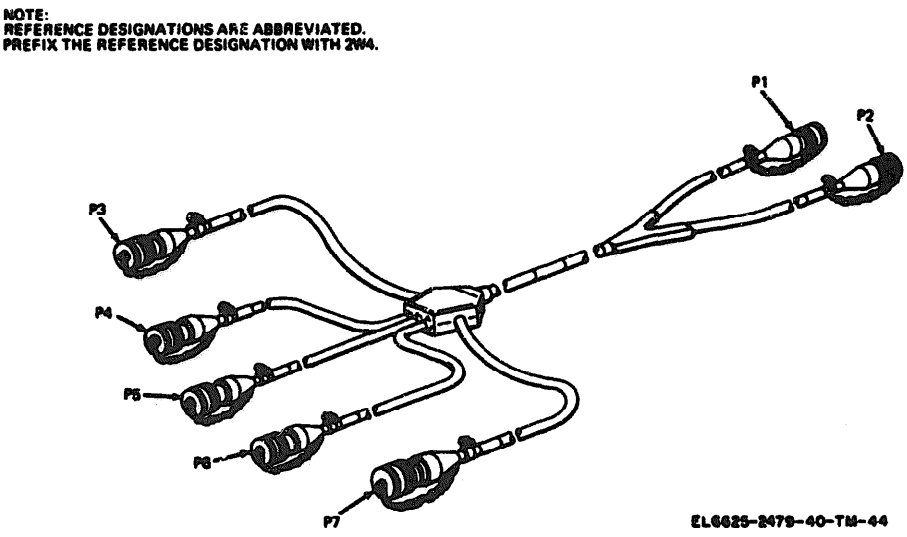

Figure 3-29. Cable Assembly, Special Purpose, Electrical, Branched CX-12717/AYM-8, parts location.

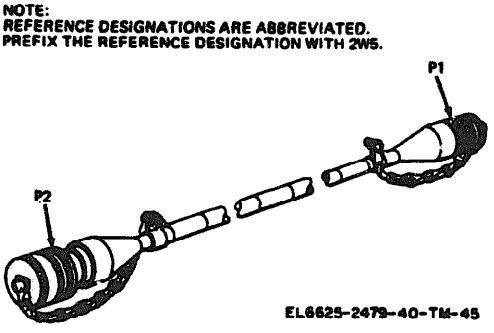

Figure 3-30. Cable Assembly, Power, Electrical CX-13714/AYM-8, parts location.

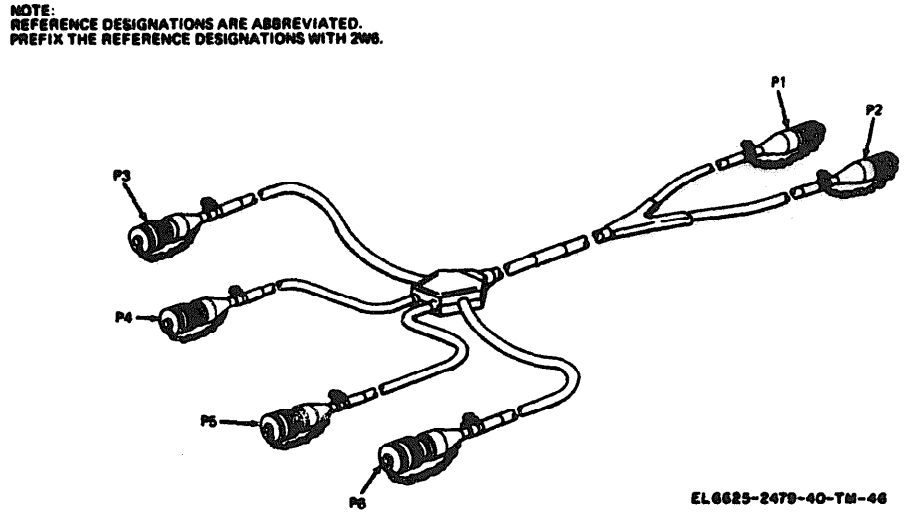

Figure 3-31. Cable Assembly, Special Purpose, Electrical Branched CX-12719/AYM-8, parts location.

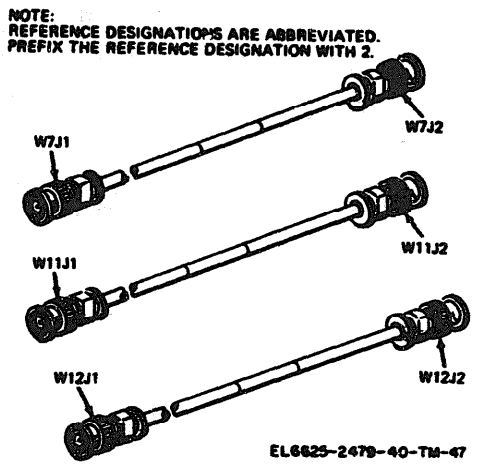

Figure 3-32. Cable Assembly, radio Frequency CG-3679/AYM-8, parts location.

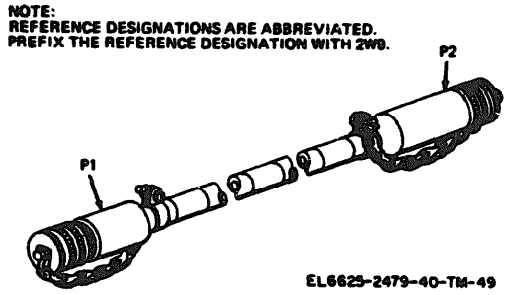

Figure 3-34. Cable Assembly, Special Purpose, Electrical CX-12721/AYM-8, parts location.

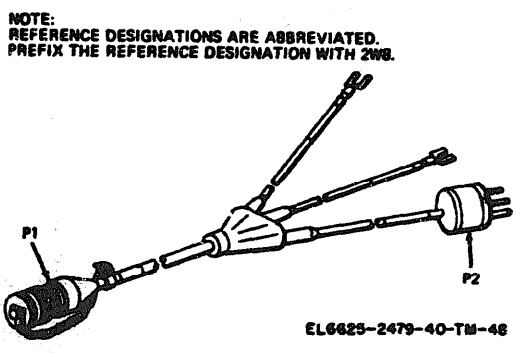

Figure 3-33. Cable Assembly, Power, Electrical, Branched CX-12724/AYM-8, parts location.

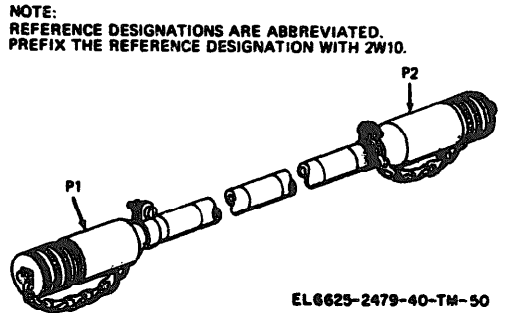

Figure 3-35. Cable Assembly, Special Purpose, Electrical CX-12722/AYM-8, part location.

Section IV. ALIGNMENT AND ADJUSTMENT

3-14. General

The alignment and adjustment procedures given here provide information for performing the following procedures within the scope of general support maintenance.

a. Plus 5 Vdc Power Supply Adjustment.

b. CRT Focus Adjustment.

c. Unblanking Adjustment.

d. Horizontal Deflection Adjustment.

3-15. Test Equipment

The following test equipments are required for aligning and adjusting the test set :

a. Differential Voltmeter ME-292 B/U.

b. Test Set, Control Monitor-Recording Head AN/AYM-9.

c. Oscilloscope AN/USM-231A.

d. Pulse Generator, HP-214A.

e. Multimeter TS-352 B/U.

f. Ratio Transformer TF-515/U.

g. Resistor, RCR32G391JR.

3-16. Preliminary Setup

Before performing alignment and adjustment procedures, remove panel assembly 1A3 from case base assembly 1A1 as described in paragraph 3-12. Place panel assembly 1A3 on a workbench in an upright position. Make switch settings and cable connections as described in the following paragraphs.

a. Set test set switches and controls to the following positions :

Switch/Control	Position
DISPLAY SELECT	IR
DIM	MIDRANGE
DATA DEMAND KA-60	OFF
DATA DEMAND IR	OFF
DATA DEMAND SLAR	OFF
DATA DEMAND KA-76	OFF
PRIORITY	KA60-1
SLAR RANGE DELAY-	0
SLAR RANGE __	25
PITCH	0'
ROLL	0"
IR FILTER	1
KA-76 ANGULAR POSITION	1
NAVIGATION DATA	111111
DATE	111111
EXPSR	1
SORTIE AND TAKING UNIT	111
FOCAL LENGTH	11
TIME	11
MODE SEL	NUM
BARO ALT	5
5VDC POWER	OFF
100 VDC POWER	OFF
28 VDC POWER	OFF
115 VAC POWER	OFF
CYCLING RATE (SWITCH)	INTERNAL
CYCLING RATE (POT)	FULL CCW

b. Connect test set cable 2W8 as follows :

(1) 2W8-P1 to 1A3J1 on test set.

(2) 2 2W8-P2 to 115 Vac, 400 Hz, single phase bench power source (power off).

(3) 2W8-E2 to 28 Vdc bench power source (power off).

(4) 2W8-E1 to 28 Vdc return.

3-17. Plus 5 Vdc Power Supply Adjustment

Adjust the +5 Vdc power supply 1A3A1 as follows :

a. Remove power supply 1A3A1 from panel assembly 1A3 (fig. 3-11) and reconnect plug 1A3-A1P1.

b. Connect the differential voltmeter (50 V range) to test set front panel test points 6A(+) and 6B(-).

WARNING

Low voltages hazardous to life exist in power supply 1A3A1 when test set power is on.

c. Set 115 VAC and 28VDC bench power source ON-OFF switches to ON positions.

d. Set 115 VAC and 5VDC switches on test set to ON positions.

e. Loosen the locknut on potentiometer 1A3-A1R7 on +5 Vdc power supply 1A3A1 and set to midrange. Rotate the potentiometer one third of its travel clockwise and counterclockwise. Throughout this range the differential voltmeter should read between +5.2 Vdc and +4.8 Vdc. Reset the potentiometer to midrange and tighten locknut.

f. Set 115 VAC and 5VDC switches on test set to OFF positions.

g. Disconnect **connector 1A8A1P1 and replace** power supply 1A3A1 **(fig. 3–11).**

3-18. CRT Focus Adjustment

Adjust CRT focus as follows:

***a.* Connect** test set cable 2W4 as shown in **figure 3–36.**

(1) 2W4-P1 to 1A3J6 on test set.

(2) 2W4-P2 to 1A3J7 on test set.

(3) 2W4-P5 to J3 on Teat Set, Control Monitor-Recording Head AN/AYM-9 (CM-RH test set).

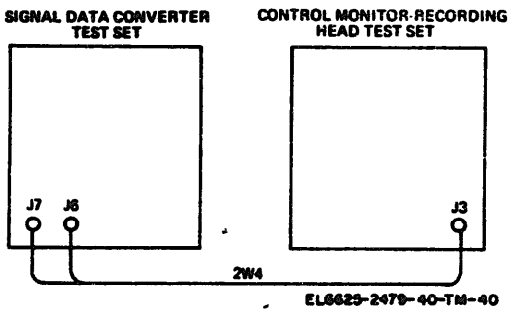

Figure 3-36. CRT focus adjustment, test setup.

b. Set the following switches/controls on the CM-RH test set to the positiona indicated below:

Switch/Control	Position
RHA TEST SELECT	KA6-0, IR/SLAR, CDM
RHA MODE	CONTINUOUS
O F F / O N	ON

***c.* Turn on CM-RH** test set by setting OFF/ ON switch to ON.

d. Adjust DIM potentiometer 1A3R5, on test set front panel, to a point that is approximately a quarter of the way down from its maximum clockwise rotational position.

e. Look for a slowly rotating circle on the face of the CRT on the teat set.

f. Remove the rear cover plate on monitor assembly 1A3A5.

WARNING

High voltages hazardous to life exist within monitor assembly 1A3A5 when it is connected to the CM-RH test set.

g. Adjust 1A3A5A1R13 for the best focus of the circle.

h. Set OFF/ON switch on the C**M-RH test** set to OFF. At the test set, set 115VAC POWER circuit breaker to OFF.

i. ~~Disconnect~~ cable 2W4 from the set **set** and **CM-RH test set.**

j. Replace the cover plate removed from monitor assembly 1A3A5.

3-19. Unblanking Adjustment

Adjust unblanking as follows:

a. Adjust pulse generator for the followin**g** output :

(1) Pulse amplitude 80 V ± 5 Vdc.

(2) Pulse width 10 μsec ±2 μsec.

(3) Repetition rate 5 kHz 0.5 kHz.

(4) Rise and fall time 2 **μsec max.**

b. Connect pulse **generator to test set front** panel test points 2A and **ground. Connect vertical input of oscilloscope to SCOPE connector** marked "Z" on **test set. Make this connection using cables 2W7, 2W11, or 2W12.**

c. Remove the rear coverplate on monitor **as**sembly 1A3A5.

d. Set the test set 115VAC and 5VDC switch**es** to ON.

e. Adjust capacitor 1A3A5A1CP7, located in the monitor assembly 1A3A5, for the best obtainable pulse, that is,

(1) Fall and rise times are less than or equal to 3 usec.

(2) Negative going rectangular pulse whose high level is between +4.0 and +5.0 Vdc and whose low level is between -0.3 and +0.3 Vdc.

f. Set the test set 115VAC and 5VDC switches to OFF position.

g. Replace the coverplate removed from monitor assembly 1A3A5.

3-20. Horizontal Deflection Adjustment

Adjust horizontal deflection as follows :

a. Adjust pulse generator using oscilloscope as a monitor for the following output:

Pulse amplitude	24.0 to 27.0 Vdc
Pulse width	30 to 34 usec
Repetition rate	45 to 55 Hz
Rise and fall time	Less than or equal to 2 usec

b. Connect pulse generator output to 1A3J7-E (reference to ground) and oscilloscope vertical

input to SCOPE X connector on test set. Use cable 2W7, 2W11, or 2W12 to connect oscilloscope to SCOPE X.

Low voltages hazardous to life exist in test set when it is connected to external primary power sources.

c. Adjust capacitor 1A8C2 for best obtainable pulse, that is, as follows:

Rise and fall time	Less than or equal to 2 μsec
Flat top response	Less than or equal to 0.2 volts
Pulse amplitude	2.2 to +2.6 Vdc
Pulse width	30 to 34 μsec

d. Remove pulse generator and oscilloscope from the test set.

Section V. REPAIR

3-21. Parts Replacement Techniques

All parts of the test set are easily accessible and can be replaced without special procedures. However, the following general practices and precautions apply to the repair of the equipment.

a. For components other than integrated circuit elements, use a 55-watt maximum capacity pencil type soldering iron to prevent damage to transistors, diodes, and similar components. If the iron is to be supplied with alternating current, use an isolating transformer between the soldering iron and the power source. Do not use a soldering gun; damaging voltages can be induced into components.

b. When soldering transistor or diode leads, solder quickly. Wherever the wiring configuration permits, use a heatsink (such as long-nosed pliers) between the soldered joint and the transistor or diode to carry away excess heat. Use approximately the same lead length on replacement parts and dress leads as original.

c. When removing integrated circuit elements, proceed as follows:

(1) Note orientation of integrated circuit element locator dot.

CAUTION

When removing leads from terminals of integrated circuit holder, be careful not to apply upward or lateral pressure to terminals and lands.

(2) Clip all 14 leads of the integrated circuit element between the terminal and the body of the chip. Lift off integrated circuit element.

(3) Using a 25-watt soldering iron and a pair of long-nosed pliers, remove those parts of the leads embedded in the holder terminals.

(4) Remove excess solder from holder and terminals by heating them with a soldering iron and removing solder with a solder sucker.

(5) Insert new integrated circuit in holder terminals in the orientation noted in step 1.

CAUTION

When soldering in a new integrated circuit element (using a 25-watt soldering iron only) be sure there is no bridging of the solder between terminals or leads.

(6) Solder leads of integrated circuit into terminals on holder.

d. Wiring diagram information and cable diagrams, figures 3–3 through 3–7 and figures FO–10 through FO–17 show details of circuit wiring for parts replacement.

3-22. Parts Substitution

Do not use parts substitution as a troubleshooting method. Substitute parts only when your analysis of the trouble clearly indicates that a specific stage or part is the likely cause of the problem.

3-23. Checkout After Repair

After repair of the test set is complete, perform the checkout procedure of paragraph 3–24.

Section VI. GENERAL SUPPORT TESTING PROCEDURES

3-24. General

a. The primary purpose of the general support testing procedures is to insure that the equipment which has been repaired is performing as it should before being returned to the users. The second purpose of the test is to serve as a basis for troubleshooting the test set (para 3–4). The test procedure is tabulated in table 3–7. For the most part the instructions you need for the test procedure are contained in the table. For a

long or involved procedure, there is a reference in the table to another **paragraph** where the **procedure** is contained. **Follow the** procedural **steps in** the order given. Remember to set the controls accurately.

b. The table is divided into five columns. The- Step no. indicates the sequence of steps in the teat. Follow this sequence. The step number also relates to the Item no. column in the trouble+ shooting chart (table Q-8). For example, if a trouble becomes evident while you are attempt+ ing step 5 of the test, look at item 5 in the trou- **bleshooting chart for the method of eliminating the trouble. The *Test equipment control settings* and test set control settings show you the proper positions for controls or switches on the external test equipment and for the test set during a particular step. The *Test procedure* column contains either step-by-step-instructions for performing the procedure involved or a reference to a paragraph which does. The *Performance standard* column shows you the indication, reading, or reaction you should get for the test you are doing. If the performance standard is not met, refer to troubleshooting.**

Table 3-7. General Support Test Procedure

Step No.	Control settings: Test equipment	Control settings: Test set	Test procedure	Performance standard
1	*Multimeter TS-686 B/U:* Resistance range: 0 to Rx1000.	N/A	Open accessory case, (unit 2) remove cable check for continuity. Inspect cables.	Continuity of cables check per paragraph 3-8.
2	N/A	a. 5 VDC POWER, 100 VDC POWER, 28 VDC POWER, and 115 VAC POWER switches to OFF.	a. Check to see that all external power supplies are off.	a. N/A.
		b. Same as step a	b. Install connector 2W8P1 to POWER IN connector 1A2J1.	b. N/A.
		c. Same as step a	c. Connect and secure terminations 2W8E1 and 2W8E2 to +28 Vdc and return lines on external 28 Vdc supply.	c. N/A.
		d. Same as step a	d. Plug connector 2W8P2 into external 115 Vac, 400 Hz, single phase power outlet.	d. N/A.
		e. Same as step a	e. Turn on external +28 Vdc supply.	e. N/A.
		f. 115 VAC POWER switch to ON	f. Observe 115 VAC POWER and 26VAC POWER lamps and ELAPSED TIME meter.	f. 115VAC POWER lamp lights. 26VAC POWER lamp lights. ELAPSED TIME meter runs.
3	N/A	28VDC POWER switch to ON	Observe 28VDC POWER lamp	28VDC POWER lamp lights.
4	N/A	100VDC POWER switch to ON	Observe 100VDC POWER lamp	100VDC POWER lamp lights.
5	N/A	5VDC POWER switch to ON	Observe 5VDC POWER lamp	5VDC POWER lamp lights.
6	*Voltmeter ME-202B/U:* Dc voltage range: 50.	NAVIGATION DATA switches: a. 10^0 at 1, all others at 0	a. Jump TEST POINTS 5D, 6B, 6D, then measure dc voltage between TEST POINT 12C (+) and 6B (−).	a. +4.5 to +5.5 Vdc.
		b. 20^0 at 2	b. Measure dc voltage between TEST POINTS 12A (+) and 6B (−).	b. +4.5 to +5.5 Vdc.
		c. 10^0 at 4	c. Measure dc voltage between TEST POINTS 12B (+) and 6B (−).	c. +4.5 to +5.5 Vdc.
		d. 10^0 at 5	d. Measure dc voltage between TEST POINTS 12D (+) and 6B (−).	d. +4.5 to +5.5 Vdc.
		e. 10^1 at 1, all others to 0	e. Measure dc voltage between TEST POINTS 13C (+) and 6B (−).	e. +4.5 to +5.5. Vdc.

	f. 10^{7} at 2	*f.* Measure dc voltage between TEST POINTS 18A (+) and 6B(−).	*f.* +4.5 to +5.5 Vdc.
	g. 10^{3} at 4	*g.* Measure dc voltage between TEST POINTS 13B (+) and 6B (−).	*g.* +4.5 to +5.5 Vdc.
	h. 10^{1} at 5	*h.* Measure dc voltage between TEST POINTS 13D (+) and 6B (−).	*h.* +4.5 to +5.5 Vdc.
	i. 10^{7} at 1, and all others at 0	*i.* Measure dc voltage between TEST POINTS 14C (+) and 6B (−).	*i.* +4.5 to +5.5 Vdc.
	j. 10^{5} at 2	*j.* Measure dc voltage between TEST POINTS 14A (+) and 6B (−).	*j.* +4.5 to +5.5 Vdc.
	k. 10^{3} at 4	*k.* Measure dc voltage between TEST POINTS 14B (+) and 6B (−).	*k.* +4.5 to +5.5 Vdc.
	l. 10^{1} at 5	*l.* Measure dc voltage between TEST POINTS 14D (+) and 6B(−).	*l.* +4.5 to +5.5 Vdc.
	m. 10^{5} at 1, all others at 0	*m.* Measure dc voltage between TEST POINTS 15C (+) and 6B(−).	*m.* +4.5 to +5.5 Vdc.
	n. 10^{3} at 2	*n.* Measure dc voltage between TEST POINTS 15A (+) and 6B (−).	*n.* +4.5 to +5.5 Vdc.
	o. 10^{1} at 4	*o.* Measure dc voltage between TEST POINTS 15B (+) and 6B (−).	*o.* +4.5 to +5.5 Vdc.
	p. 10^{7} at 5	*p.* Measure dc voltage between TEST POINTS 15D (+) and 6B (−).	*p.* +4.5 to +5.5 Vdc.
	q. 10^{4} at 1, all others at 0	*q.* Measure dc voltage between TEST POINTS 16C (+) and 6B (--).	*q.* +4.5 to +5.5 Vdc.
	r. 10^{2} at 2	*r.* Measure dc voltage between TEST POINTS 16A (+) and 6B(−).	*r.* +4.5 to +5.5 Vdc.
	s. 10^{0} at 4	*s.* Measure dc voltage between TEST POINTS 16B (+) and 6B (−).	*s.* +4.5 to +5.5 Vdc.
	t. 10^{6} at 5	*t.* Measure dc voltage between TEST POINTS 16D (+) and 6B (−).	*t.* +4.5 to +5.5 Vdc.
	u. 10^{5} at 1, all others at 0	*u.* Measure dc voltage between TEST POINTS 17C (+) and 6B(−).	*u.* +4.5 to +5.5 Vdc.

Step No.	Control settings: Test equipment	Control settings: Test set	Test procedure	Performance standard
		v. 10⁵ at 2	v. Measure dc voltage between TEST POINTS 17A (+) and 6B (−).	v. +4.5 to +5.5 Vdc.
		w. 10⁵ at 4	w. Measure dc voltage between TEST POINTS 17B (+) and 6B (−).	w. +4.5 to +5.5 Vdc.
		x. 10⁵ at 5	x. Measure dc voltage between TEST POINTS 17D (+) and 6B (−).	x. +4.5 to +5.5 Vdc.
		y. Set all NAVIGATION DATA thumb wheels to 0.	y. Remove jumpers	y. N/A.
7	*Voltmeter ME-602 B/U:* De voltage range: 50.	a. FOCAL LENGTH switches to 00	a. Remove cover from CONTROL MONITOR connector J3. Jumper pin X of J3 to TEST POINT 6D (signal ground).	a. N/A.
		b. FOCAL LENGTH switches to 01	b. Measure dc voltage between J3-e (+) and TEST POINT 6B (−).	b. +4.5 to +5.5 Vdc.
		c. FOCAL LENGTH switches to 02	c. Measure dc voltage between J3-Y (+) and TEST POINT 6B (−).	c. +4.5 to +5.5 Vdc.
		d. FOCAL LENGTH switches to 03	d. Measure dc voltage between J3-b (+) and TEST POINT 6B (−).	d. +4.5 to +5.5 Vdc.
		e. FOCAL LENGTH switches to 05	e. Measure dc voltage between J3-h (+) and TEST POINT 6B (−).	e. +4.5 to +5.5 Vdc.
		f. Same as Step e	f. Remove jumper and reconnect between J3-e and TEST POINT 6D.	f. N/A.
		g. FOCAL LENGTH switches to 10	g. Measure dc voltage between J3-e and TEST POINT 6B (−).	g. +4.5 to +5.5 Vdc.
		h. FOCAL LENGTH switches to 20	h. Measure dc voltage between J3-Y (+) and TEST POINT 6B (−).	h. +4.5 to +5.5 Vdc.
		i. FOCAL LENGTH switches to 30	i. Measure dc voltage between J3-b (+) and TEST POINT 6B (−).	i. +4.5 to +5.5 Vdc.
		j. FOCAL LENGTH switches to 50	j. Measure dc voltage between J3-h (+) and TEST POINT 6B (−).	j. +4.5 to +5.5 Vdc.
		k. FOCAL LENGTH switches to 00	k. Remove jumper. Remove voltmeter. Replace cap on J3.	k. N/A.

8	a. Set decade resistor to 390 ohms. b. *Oscilloscope AN/USM-281A:* SYNC to INT (+).	a. FOCAL LENGTH switches to 00 b. Same as step a c. DATA DEMAND KA-60 switch to CONTINUOUS DISPLAY. PRIORITY switch to KA60-1.	a. Connect decade resistor across TEST POINTS 6B and 18D. b. Place vertical input of oscilloscope across TEST POINT 6B (−) and TEST POINT 9C (probe). c. Observe waveshape on oscilloscope.	a. N/A. b. N/A. c. Waveshape characteristics, (A, fig. 3-1): (1) Amplitude: +2.2 to +4.0 Vdc. (2) Width: 400 to 800 μsec. (3) Rise time: 75 μsec max. (4) Period: 70 msec.
9	Same as step 8	DATA DEMAND KA-60 switch to SINGLE PULSE.	Depress PULSE switch and observe a single pulse. Repeat as required.	Same as 8c, except is single pulse.
10	Same as step 8	PRIORITY switch to KA60-2	a. Place vertical input of oscilloscope across TEST POINT 6B (−) and J5-*x* (probe). b. Depress PULSE switch and observe a single pulse. Repeat if required.	a. N/A. b. Same as 8c, except is single pulse.
11	Same as step 8	DATA DEMAND KA-60 switch to CONTINUOUS DISPLAY.	a. Observe waveshape on oscilloscope. b. Disconnect decade resistor	a. Same as 8c. b. N/A.
12	*Oscilloscope AN/USM-281A:* SYNC to INT (+).	a. DATA DEMAND KA-60 switch to OFF. DATA DEMAND-IR switch to CONTINUOUS DISPLAY. b. Same as step a	a. Jump TEST POINTS 5D, 6B, 6D. Connect oscilloscope probe return at TEST POINT 6B and oscilloscope probe to TEST POINT 9A. b. Observe waveshape on oscilloscope.	Waveshape characteristics, (E, fig. 3-1): (1) Amplitude: 22 to 32 Vdc. (2) Width: 25 to 55 milliseconds. (3) Rise time: 15 μsec max. (4) Period: 70 msec.
13	Same as step 12	DATA DEMAND-IR switch to SINGLE PULSE.	Depress PULSE switch while observing waveshape on oscilloscope. Repeat if required.	A single pulse (amplitude of +23 to +31 Vdc) which rises when PULSE switch is depressed and falls when PULSE switch is released (H, fig. 3-1).
14	Same as step 12	a. DATA DEMAND-IR switch to OFF. DATA DEMAND-SLAR switch to CONTINUOUS DISPLAY. b. N/A	a. Move oscilloscope probe from TEST POINT 9A to TEST POINT 9B. b. Observe waveshape on oscilloscope.	a. N/A. b. Waveshape characteristics (C, fig. 3-1): (1) Amplitude: +22 to +32 Vdc.

Step No.	Control settings: Test equipment	Control settings: Test set	Test procedure	Performance standard
				(2) Width: 25 to 55 milliseconds. (3) Rise time: 15 μsec max. (4) Period: 70 msec.
15	Same as step 12	DATA DEMAND-SLAR switch to SINGLE PULSE.	Depress PULSE switch while observing waveshape on oscilloscope. Repeat if required.	A single pulse (amplitude c[illegible]23 to +31 Vdc) which rises when PULSE switch is depressed and falls when PULSE switch is released (D, fig. 3-1).
16	Same as step 12	*a.* DATA DEMAND-SLAR switch to OFF. DATA DEMAND KA-76 switch to CONTINUOUS DISPLAY.	*a.* Move oscilloscope probe from TEST POINT 9B to TEST POINT 9D.	*a.* N/A.
		b. Same as step *a*	*b.* Observe waveshape on oscilloscope.	*b.* Waveshape characteristics, (G, fig. 3-1): (1) Amplitude: +22 to +32 Vdc. (2) Width: 8 to 32 milliseconds. (3) Rise time: 15 μsec max. (4) Period: 70 msec.
17	Same as step 12	*a.* DATA DEMAND KA-76 switch to SINGLE PULSE.	*a.* Depress PULSE switch while observing waveshape on oscilloscope. Repeat if required.	*a.* A single pulse with the following characteristics, (H, fig. 3-1): (1) Amplitude: +22 to +32 Vdc. (2) Width: 8 to 32 milliseconds. (3) Rise time: 15 μsec max.
		b. DATA DEMAND KA-76 switch to OFF.	*b.* N/A	*b.* N/A.
18	*Pulse Generator SG-4-81: Oscilloscope AN/USM-281A:* SYNC to INT (+).	*a.* DATA DEMAND KA-76 switch to SINGLE PULSE.	*a.* Connect output of pulse generator to oscilloscope channel A.	*a.* N/A.
		b. Same as step *a*	*b.* Adjust output of pulse generator, as seen on oscilloscope to be as follows: (1) Amplitude: +4.8 to +5.2 Vdc. (2) Width: 30 to 34 μsec. (3) Rise time: 0.8 to 1.2 μsec. (4) Fall time: 0.8 to 1.2 μsec. (5) Period: 730 to 790 μsec.	*b.* N/A.
		c. Same as step *a*	*c.* Jumper TEST POINTS 11A, 11B, and 11C. Connect output of pulse generator to TEST POINT 11A.	*c.* N/A.
		d. Same as step *a*	*d.* Connect channel B of oscilloscope to TEST POINT 6C.	*d.* N/A.

		c. Same as step c	c. Observe waveforms	c. Channel B waveform characteristics: (1) Amplitude: 4.0 to 6.0 Vdc. (2) Width: 7 to 27 μsec. (3) Rise time: 3 μsec max. (4) Period: 680 to 840 μsec. (5) When compared to CHANNEL A waveform, CHANNEL B waveform starts with delay of between 300 to 600 μsec.
		f. DATA DEMAND KA-76 switch to OFF.	f. Remove jumper wires, pulse generator, and oscilloscope connections to test set.	f. N/A.
19	*Voltmeter ME-202B/U:* Dc voltage range: 50.	a. (1) DATE-DAY switches at 40. (2) 115VAC POWER switch to OFF. (3) 115VAC POWER switch to ON. (4) N/A	a. N/A (2) Connect jumper between TEST POINTS 6A and 18B. (3) N/A. (4) Connect jumper between CONTROL MONITOR connector J3 pin R and TEST POINT 6B (gnd).	a. N/A.
		b. Same as step a	b. (1) Measure dc voltage between J3-B and TEST POINT 6B. (2) Measure dc voltage between J3-C and TEST POINT 6B. (3) Measure dc voltage between J3-D and TEST POINT 6B. (4) Measure dc voltage between J3-E and TEST POINT 6B. (5) Measure dc voltage between J3-F and TEST POINT 6B. (6) Measure dc voltage between J3-G and TEST POINT 6B. (7) Measure dc voltage between J3-H and TEST POINT 6B. (8) Measure dc voltage between J3-J and TEST POINT 6B.	b. (1) +4.5 to +5.5 Vdc. (2) +4.5 to +5.5 Vdc. (3) +4.5 to +5.5 Vdc. (4) +4.5 to +5.5 Vdc. (5) +4.5 to +5.5 Vdc. (6) +4.5 to +5.5 Vdc. (7) +4.5 to +5.5 Vdc. (8) +4.5 to +5.5 Vdc.

Step No	Control settings: Test equipment	Control settings: Test set	Test procedure	Performance standard
			(9) Measure dc voltage between J3–K and TEST POINT 6B.	(9) +4.5 to +5.5 Vdc.
			(10) Measure dc voltage between J3–L and TEST POINT 6B.	(10) +4.5 to +5.5 Vdc.
		c. DATE-DAY switches to 00	*c.* Measure dc voltage between J3–B and TEST POINT 6B.	*c.* Zero Vdc.
		d. DATE-DAY switches to 10	*d.* Measure dc voltage between J3–C and TEST POINT 6B.	*d.* Zero Vdc.
		e. DATE-DAY switches to 20	*e.* Measure dc voltage between J3–D and TEST POINT 6B.	*e.* Zero Vdc.
		f. DATE-DAY switches to 30	*f.* Measure dc voltage between J3–E and TEST POINT 6B.	*f.* Zero Vdc.
		g. DATE-DAY switches to 00	*g.* Remove jumper and reconnect to J3–S.	*g.* N/A.
		h. N/A	*h.* Measure dc voltage between J3–B and TEST POINT 6B.	*h.* Zero Vdc.
		i. DATE-DAY switches to 01	*i.* Measure dc voltage between J3–C and TEST POINT 6B.	*i.* Zero Vdc.
		j. DATE-DAY switches to 02	*j.* Measure dc voltage between J3–D and TEST POINT 6B.	*j.* Zero Vdc.
		k. DATE-DAY switches to 03	*k.* Measure dc voltage between J3–E and TEST POINT 6B.	*k.* Zero Vdc.
		l. DATE-DAY switches to 04	*l.* Measure dc voltage between J3–F and TEST POINT 6B.	*l.* Zero Vdc.
		m. DATE-DAY switches to 05	*m.* Measure dc voltage between J3–G and TEST POINT 6B.	*m.* Zero Vdc.
		n. DATE-DAY switches to 06	*n.* Measure dc voltage between J3–H and TEST POINT 6B.	*n.* Zero Vdc.
		o. DATE-DAY switches to 07	*o.* Measure dc voltage between J3–J and TEST POINT 6B.	*o.* Zero Vdc.
		p. DATE-DATE switches to 08	*p.* Measure dc voltage between J3–K and TLST POINT 6B.	*p.* Zero Vdc.
		q. DATE-DAY switches to 09	*q.* Measure dc voltage between J3–L and TEST POINT 5B.	*q.* Zero Vdc.
20	Same as step 19	*a.* Set DATE-MONTH switches to 00.	*a.* Remove jumper from J3–S and reconnect to J3–T.	*a.* N/A.
		b. Same as step *a*	*b.* Measure dc voltage between J3–B and TEST POINT 6B.	*b.* Zero Vdc.
		c. Set DATE-MONTH switches to 10.	*c.* Measure dc voltage between J3–C and TEST POINT 6B.	*c.* Zero Vdc.
		d. Set DATE-MONTH switches to 00.	*d.* Remove jumper from J3–T and reconnect to J3–U.	*d.* N/A.

		a. Same as step a	a. Measure dc voltage between J3–B and TEST POINT 6B.	a. Zero Vdc.
		f. Set DATE-MONTH switches to 01.	f. Measure dc voltage between J3–C and TEST POINT 6B.	f. Zero Vdc.
		g. Set DATE-MONTH switches to 02.	g. Measure dc voltage between J3–D and TEST POINT 6B.	g. Zero Vdc.
		h. Set DATE-MONTH switches to 03.	h. Measure dc voltage between J3–E and TEST POINT 6B.	h. Zero Vdc.
		i. Set DATE-MONTH switches to 04.	i. Measure dc voltage between J3–F and TEST POINT 6B.	i. Zero Vdc.
		j. Set DATE-MONTH switches to 05.	j. Measure dc voltage between J3–G and TEST POINT 6B.	j. Zero Vdc.
		k. Set DATE-MONTH switches to 06.	k. Measure dc voltage between J3–H and TEST POINT 6B.	k. Zero Vdc.
		l. Set DATE-MONTH switches to 07.	l. Measure dc voltage between J3–J and TEST POINT 6B.	l. Zero Vdc.
		m. Set DATE-MONTH switches to 08.	m. Measure dc voltage between J3–K and TEST POINT 6B.	m. Zero Vdc.
		n. Set DATE-MONTH switches to 09.	n. Measure dc voltage between J3–L and TEST POINT 6B.	n. Zero Vdc.
21	Same as step 19	a. Set DATE-YEAR switches to 00	a. Remove jumper from J3–U and reconnect to J3–V.	a. N/A.
		b. Same as step a	b. Measure dc voltage between J3–B and TEST POINT 6B.	b. Zero Vdc.
		c. Set DATE-YEAR switches to 10	c. Measure dc voltage between J3–C and TEST POINT 6B.	c. Zero Vdc.
		d. Set DATE-YEAR switches to 20	d. Measure dc voltage between J3–D and TEST POINT 6B.	d. Zero Vdc.
		e. Set DATE-YEAR switches to 30	e. Measure dc voltage between J3–E and TEST POINT 6B.	e. Zero Vdc.
		f. Set DATE-YEAR switches to 40	f. Measure dc voltage between J3–F and TEST POINT 6B.	f. Zero Vdc.
		g. Set DATE-YEAR switches to 50	g. Measure dc voltage between J3–G and TEST POINT 6B.	g. Zero Vdc.
		h. Set DATE-YEAR switches to 60	h. Measure dc voltage between J3–H and TEST POINT 6B.	h. Zero Vdc.
		i. Set DATE-YEAR switches to 70	i. Measure dc voltage between J3–J and TEST POINT 6B.	i. Zero Vdc.
		j. Set DATE-YEAR switches to 80	j. Measure dc voltage between J3–K and TEST POINT 6B.	j. Zero Vdc.
		k. Set DATE-YEAR switches to 90	k. Measure dc voltage between J3–L and TEST POINT 6B.	k. Zero Vdc.
		l. Set DATE-YEAR switches to 00	l. Remove jumper from J3–V and reconnect to J3–W.	l. N/A.

o.	Control settings: Test equipment	Control settings: Test set	Test procedure	Performance standard
		m. Same as step *l*	*m.* Measure dc voltage between J3–B and TEST POINT 6B.	*m.* Zero Vdc.
		n. Set DATE-YEAR switches to 01	*n.* Measure dc voltage between J3–C and TEST POINT 6B.	*n.* Zero Vdc.
		o. Set DATE-YEAR switches to 02	*o.* Measure dc voltage between J3–D and TEST POINT 6B.	*o.* Zero Vdc.
		p. Set DATE-YEAR switches to 03	*p.* Measure dc voltage between J3–E and TEST POINT 6B.	*p.* Zero Vdc.
		q. Set DATE-Year switches to 04	*q.* Measure dc voltage between J3–F and TEST POINT 6B.	*q.* Zero Vdc.
		r. Set DATE-YEAR switches to 05	*r.* Measure dc voltage between J3–G and TEST POINT 6B.	*r.* Zero Vdc.
		s. Set DATE-YEAR switches to 06	*s.* Measure dc voltage between J3–H and TEST POINT 6B.	*s.* Zero Vdc.
		t. Set DATE-YEAR switches to 07	*t.* Measure dc voltage between J3–J and TEST POINT 6B.	*t.* Zero Vdc.
		u. Set DATE-YEAR switches to 08	*u.* Measure dc voltage between J3–K and TEST POINT 6B.	*u.* Zero Vdc.
		v. Set DATE-YEAR switches to 09	*v.* Measure dc voltage between J3–L and TEST POINT 6B.	*v.* Zero Vdc.
	Same as step 19	*a.* Set SORTIE AND TAKING UNIT switches to 000.	*a.* Remove jumper from J3–W and reconnect to J3–M.	*a.* N/A.
		b. Same as step *a*	*b.* Measure dc voltage between J3–B and TEST POINT 6B.	*b.* Zero Vdc.
		c. Set SORTIE AND TAKING UNIT switches to 100.	*c.* Measure dc voltage between J3–C and TEST POINT 6B.	*c.* Zero Vdc.
		d. Set SORTIE AND TAKING UNIT switches to 200.	*d.* Measure dc voltage between J3–D and TEST POINT 6B.	*d.* Zero Vdc.
		e. Set SORTIE AND TAKING UNIT switches to 300.	*e.* Measure dc voltage between J3–E and TEST POINT 6B.	*e.* Zero Vdc.
		f. Set SORTIE AND TAKING UNIT switches to 400.	*f.* Measure dc voltage between J3–F and TEST POINT 6B.	*f.* Zero Vdc.
		g. Set SORTIE AND TAKING UNIT switches to 500.	*g.* Measure dc voltage between J3–G and TEST POINT 6B.	*g.* Zero Vdc.
		h. Set SORTIE AND TAKING UNIT switches to 600.	*h.* Measure dc voltage between J3–H and TEST POINT 6B.	*h.* Zero Vdc.
		i. Set SORTIE AND TAKING UNIT switches to 700.	*i.* Measure dc voltage between J3–J and TEST POINT 6B.	*i.* Zero Vdc.
		j. Set SORTIE AND TAKING UNIT switches to 800.	*j.* Measure dc voltage between J3–K and TEST POINT 6B.	*j.* Zero Vdc.
		k. Set SORTIE AND TAKING UNIT switches to 900.	*k.* Measure dc voltage between J3–L and TEST POINT 6B.	*k.* Zero Vdc.

	l. Set SORTIE AND TAKING UNIT switches to 000.	*l.* Remove jumper from J3-M and reconnect to J3-N.	*l.* N/A.
	m. N/A	*m.* Measure dc voltage between J3-B and TEST POINT 6B.	*m.* Zero Vdc.
	n. Set SORTIE AND TAKING UNIT switches to 010.	*n.* Measure dc voltage between J3-C and TEST POINT 6B.	*n.* Zero Vdc.
	o. Set SORTIE AND TAKING UNIT switches to 020.	*o.* Measure dc voltage between J3-D and TEST POINT 6B.	*o.* Zero Vdc.
	p. Set SORTIE AND TAKING UNIT switches to 030.	*p.* Measure dc voltage between J3-E and TEST POINT 6B.	*p.* Zero Vdc.
	q. Set SORTIE AND TAKING UNIT switches to 040.	*q.* Measure dc voltage between J3-F and TEST POINT 6B.	*q.* Zero Vdc.
	r. Set SORTIE AND TAKING UNIT switches to 050.	*r.* Measure dc voltage between J3-G and TEST POINT 6B.	*r.* Zero Vdc.
	s. Set SORTIE AND TAKING UNIT switches to 060.	*s.* Measure dc voltage between J3-H and TEST POINT 6B.	*s.* Zero Vdc.
	t. Set SORTIE AND TAKING UNIT switches to 070.	*t.* Measure dc voltage between J3-J and TEST POINT 6B.	*t.* Zero Vdc.
	u. Set SORTIE AND TAKING UNIT switches to 080.	*u.* Measure dc voltage between J3-K and TEST POINT 6B.	*u.* Zero Vdc.
	v. Set SORTIE AND TAKING UNIT switches to 090.	*v.* Measure dc voltage between J3-L and TEST POINT 6B.	*v.* Zero Vdc.
	w. Set SORTIE AND TAKING UNIT switches to 000.	*w.* Remove jumper from J3-N and connect to J3-P.	*w.* N/A.
	x. Same as step *w*	*x.* Measure dc voltage between J3-B and TEST POINT 6B.	*x.* Zero Vdc.
	y. Set SORTIE AND TAKING UNIT switches to 001.	*y.* Measure dc voltage between J3-C and TEST POINT 6B.	*y.* Zero Vdc.
	z. Set SORTIE AND TAKING UNIT switches to 002.	*z.* Measure dc voltage between J3-D and TEST POINT 6B.	*z.* Zero Vdc.
	aa. Set SORTIE AND TAKING UNIT switches to 003.	*aa.* Measure dc voltage between J3-E and TEST POINT 6B.	*aa.* Zero Vdc.
	ab. Set SORTIE AND TAKING UNIT switches to 004.	*ab.* Measure dc voltage between J3-F and TEST POINT 6B.	*ab.* Zero Vdc.
	ac. Set SORTIE AND TAKING UNIT switches to 005.	*ac.* Measure dc voltage between J3-G and TEST POINT 6B.	*ac.* Zero Vdc.
	ad. Set SORTIE AND TAKING UNIT switches to 006.	*ad.* Measure dc voltage between J3-H and TEST POINT 6B.	*ad.* Zero Vdc.
	ae. Set SORTIE AND TAKING UNIT switches to 007.	*ae.* Measure dc voltage between J3-J and TEST POINT 6B.	*ae.* Zero Vdc.
	af. Set SORTIE AND TAKING UNIT switches to 008.	*af.* Measure dc voltage between J3-K and TEST POINT 6B.	*af.* Zero Vdc.
	ag. Set SORTIE AND TAKING UNIT switches to 009.	*ag.* Measure dc voltage between J3-L and TEST POINT 6B.	*ag.* Zero Vdc.
	ah. Same as step *ag*	*ah.* Remove jumper from connector J3 pin P and voltmeter.	*ah.* N/A.

Step No.	Control settings: Test equipment	Control settings: Test set	Test procedure	Performance standard
23	*Voltmeter ME-202 B/U:* Dc voltage range: 50.	*a.* Set SORTIE AND TAKING UNIT switches to 009.	*a.* Measure dc voltage between J3-p and TEST POINT 6B.	*a.* +4.5 to +5.5 Vdc.
		b. Same as step *a*	*b.* Measure dc voltage between J3-n and TEST POINT 6B.	*b.* +4.5 to +5.5 Vdc.
		c. Same as step *a*	*c.* Measure dc voltage between J3-m and TEST POINT 6B.	*c.* +4.5 to +5.5 Vdc.
		d. Same as step *a*	*d.* Connect a jumper between RHA IN connector J7-H AND TEST POINT 6B.	*d.* N/A.
		e. Set EXPSR switch to 1	*e.* Measure dc voltage between J3-p and TEST POINT 6B.	*e.* Zero Vdc.
		f. Set EXPSR switch to 2	*f.* Measure dc voltage between J3-n and TEST POINT 6B.	*f.* Zero Vdc.
		g. Set EXPSR switch to 4	*g.* Measure dc voltage between J3-m and TEST POINT 6B.	*g.* Zero Vdc.
		h. Same as step *g*	*h.* Remove jumper and voltmeter connections.	*h.* N/A.
		i. Set all POWER switches to OFF	*i.* N/A	*i.* N/A.
24	*Multimeter TS-352B/U:* Resistance range: Rx1000.	*a.* Set EXPSR switch to 4	*a.* Measure resistance between CONTROL MONITOR connector J3-Z and TEST POINT 6B (ground).	*a.* Infinite resistance.
		b. Same as step *a*	*b.* Measure resistance between J3-a and TEST POINT 6B.	*b.* Infinite resistance.
		c. Same as step *a*	*c.* Measure resistance between J3-c and TEST POINT 6B.	*c.* Infinite resistance.
		d. Same as step *a*	*d.* Measure resistance between J3-d and TEST POINT 6B.	*d.* Infinite resistance.
		e. Same as step *a*	*e.* Measure resistance between J3-f and TEST POINT 6B.	*e.* Infinite resistance.
		f. Same as step *a*	*f.* Measure resistance between J3-g and TEST POINT 6B.	*f.* Infinite resistance.
		g. Same as step *a*	*g.* Measure resistance between J3-i and TEST POINT 6B.	*g.* Infinite resistance.
		h. Same as step *a*	*h.* Measure resistance between J3-j and TEST POINT 6B.	*h.* Infinite resistance.
		i. Same as step *a*	*i.* Connect a jumper between RHA IN connector J7-L and TEST POINT 6B.	*i.* N/A.
		j. Set TIME switches to 44	*j.* Measure resistance between J3-Z and TEST POINT 6B.	*j.* Zero ohms (approx).
		k. Same as step *j*	*k.* Measure resistance between J3-a and TEST POINT 6B.	*k.* Zero ohms (approx).

		l. Same as step j	l. Measure resistance between J3–c and TEST POINT 6B.	l. Zero ohms (approx).
		m. Same as step j	m. Measure resistance between J3–f and TEST POINT 6B.	m. Zero ohms (approx).
		n. Same as step j	n. Measure resistance between J3–g and TEST POINT 6B.	n. Zero ohms (approx).
		o. Same as step j	o. Measure resistance between J3–i and TEST POINT 6B.	o. Zero ohms (approx).
		p. Set TIME switches to 55	p. Measure resistance between J3–d and TEST POINT 6B.	p. Zero ohms (approx).
		q. Same as step p	q. Measure resistance between J3–j and TEST POINT 6B.	q. Zero ohms (approx).
		r. Same as step p	r. Remove jumper from J7–L and reconnect to J7–H.	r. N/A.
		s. Same as step p	s. Measure resistance between J3–J and TEST POINT 6B.	s. 3K to 5K ohms.
		t. Depress and hold TIME SET switch.	t. Measure resistance between J3–j and TEST POINT 6B.	t. Zero ohms (approx).
		u. Release TIME SET switch	u. Measure resistance between J7–M and TEST POINT 6B.	u. Zero ohms (approx).
		v. Same as step p	v. Remove jumper and voltmeter	v. N/A.
25	None	Set all POWER switches to ON	a. N/A	a. All power lamps light.
			b. Connect jumper between TEST POINTS 6A and 18B.	b. N/A.
			c. Depress FRAME NO RESET switch.	c. LAMP TEST NO GO lamp lights.
			d. Release FRAME NO RESET switch.	d. LAMP TEST NO GO lamp goes out.
26	*Voltmeter ME–202 B/U:* De voltage range: 50.	a. Same as step 25a	a. Measure dc voltage between RHA IN connector J7–V (+) and J7–G (–). Remove voltmeter leads.	a. +4.5 to +5.5 Vdc.
		b. Set 5VDC POWER switch to OFF	b. N/A	b. N/A.
		c. Depress and hold TEST switch	c. N/A	c. N/A.
		d. Set 5VDC POWER switch to ON.	d. Measure dc voltage	d. +4.5 to +5.5 Vdc.
		e. Release TEST switch	e. Remove voltmeter leads	e. N/A.
		f. Set all POWER switches to OFF.	f. Remove all jumpers	f. N/A.
27	*Multimeter TS–352 B/U:* Resistance range: Rx1000.	a. Set MODE SEL switch to ALTN	a. Measure continuity between RHA IN connector J7–X and TEST POINT 6B.	a. Open circuit.
		b. Same as step a	b. Measure continuity between J7–W and TEST POINT 6B.	b. Open circuit.

Step No.	Control settings: Test equipment	Control settings: Test set	Test procedure	Performance standard
		c. Set MODE SEL switch to BCD	*c.* Measure continuity between J7–W and TEST POINT 6B.	*c.* Short circuit (continuity).
		d. Set MODE SEL switch to NUM	*d.* Measure continuity between J7–X and TEST POINT 6B.	*d.* Short circuit (continuity).
		e. Same as step *d*	*e.* Remove multimeter leads	*e.* N/A.
28	*Voltmeter ME–202 B/U:* Dc voltage range: 50.	*a.* Set IR FILTER switch to 1 and all POWER switches to ON.	*a.* Jumper TEST POINTS 5D and 6D to EXT GND.	*a.* N/A.
		b. Set KA–76 ANGULAR POSITION switch to 3.	*b.* Measure dc voltage between SIGNALS connector J5–GG and TEST POINT 5D (–).	*b.* +24 to +30 Vdc.
		c. Same as step *b*	*c.* Measure dc voltage between J5–FF and TEST POINT 5D.	*c.* +24 to +30 Vdc.
		d. Same as step *b*	*d.* Measure dc voltage between J5–EE and TEST POINT 5D.	*d.* +24 to +30 Vdc.
		e. Same as step *b*	*e.* Measure dc voltage between J5–DD and TEST POINT 5D.	*e.* +24 to +30 Vdc.
		f. Set KA–76 ANGULAR POSITION switch to 5.	*f.* Measure dc voltage between J5–DD and TEST POINT 5D.	*f.* Zero Vdc.
		g. Set KA–76 ANGULAR POSITION switch to 4	*g.* Measure dc voltage between J5–EE and TEST POINT 5D.	*g.* Zero Vdc.
		h. Set KA–76 ANGULAR POSITION switch to 2.	*h.* Measure dc voltage between J5–FF and TEST POINT 5D.	*h.* Zero Vdc.
		i. Set KA–76 ANGULAR POSITION switch to 1.	*i.* Measure dc voltage between J5–GG and TEST POINT 5D.	*i.* Zero Vdc.
29	*Voltmeter ME–202 B/U:* Dc voltage range: 50.	*a.* Same as step 28	*a.* Measure dc voltage between SIGNALS connector J4–a (+) and TEST POINT 5D (–).	*a.* Zero Vdc.
		b. Same as step *a*	*b.* Measure dc voltage between J4–b and TEST POINT 5D.	*b.* +24 to +30 Vdc.
		c. Same as step *a*	*c.* Measure dc voltage between J4–c and TEST POINT 5D.	*c.* +24 to +30 Vdc.
		d. Same as step *a*	*d.* Measure dc voltage between J4–d and TEST POINT 5D.	*d.* +24 to +30 Vdc.
		e. Same as step *a*	*e.* Measure dc voltage between J4–e and TEST POINT 5D.	*e.* +24 to +30 Vdc.

		f. Set IR FILTER switch to 2	f. Measure dc voltage between J4-b and TEST POINT 5D.	f. Zero Vdc.
		g. Set IR FILTER switch to 3	g. Measure dc voltage between J4-c and TEST POINT 5D.	g. Zero Vdc.
		h. N/A	h. Measure dc voltage between SIGNALS connector J5-n and TEST POINT 5D.	h. Zero Vdc.
		i. Set IR FILTER switch to 4	i. Measure dc voltage between SIGNALS connector J4-d and TEST POINT 5D.	i. Zero Vdc.
		j. Set IR FILTER switch to 5	j. Measure dc voltage between J4-e and TEST POINT 5D.	j. Zero Vdc.
		k. Set IR FILTER switch to 1	k. Remove voltmeter leads	k. N/A.
30	*Voltmeter ME-202 B/U:* Dc voltage range: 50.	a. Set SLAR RANGE switch to 25	a. Measure dc voltage between J4-C and TEST POINT 5D (-).	a. +24 to +30 Vdc.
		b. Same as step a	b. Measure dc voltage between J4-B and TEST POINT 5D.	b. Zero Vdc.
		c. Same as step a	c. Measure dc voltage between J4-a and TEST POINT 5D.	c. Zero Vdc.
		d. Set SLAR RANGE switch to 50	d. Measure dc voltage between J4-C and TEST POINT 5D.	d. Zero Vdc.
		e. Same as step d	e. Measure dc voltage between J4-B and TEST POINT 5D.	e. +24 to +30 Vdc.
		f. Set SLAR RANGE switch to 99	f. Measure dc voltage between J4-B and TEST POINT 5D.	f. +24 to +30 Vdc.
		g. Same as step a	g. Remove voltmeter leads	g. N/A.
31	*Voltmeter ME-202 B/U:* Dc voltage range: 50.	a. Set SLAR RANGE DELAY switch to 0.	a. Measure dc voltage between J4-K and TEST POINT 5D.	a. +24 to +30 Vdc.
		b. Same as step a	b. Measure dc voltage between J4-J and TEST POINT 5D.	b. Zero Vdc.
		c. Same as step a	c. Measure dc voltage between J4-H and TEST POINT 5D.	c. Zero Vdc.
		d. Same as step a	d. Measure dc voltage between J4-G and TEST POINT 5D.	d. Zero Vdc.
		e. Same as step a	e. Measure dc voltage between J4-F and TEST POINT 5D.	e. Zero Vdc.
		f. Same as step a	f. Measure dc voltage between J4-E and TEST POINT 5D.	f. Zero Vdc.
		g. Same as step a	g. Measure dc voltage between J4-D and TEST POINT 5D.	g. Zero Vdc.
		h. Set SLAR RANGE DELAY switch to 10.	h. Measure dc voltage between J4-K and TEST POINT 5D.	h. Zero Vdc.
		i. Same as step a.	i. Measure dc voltage between J4-J and TEST POINT 5D.	i. +24 to +30 Vdc.

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Step No.	Control settings: Test equipment	Control settings: Test set	Test procedure	Performance standard
		j. Set SLAR RANGE DELAY switch to 20.	*j.* Measure dc voltage between J4–H and TEST POINT 5D.	*j.* +24 to +30 Vdc.
		k. Set SLAR RANGE DELAY switch to 30.	*k.* Measure dc voltage between J4–G and TEST POINT 5D.	*k.* +24 to +30 Vdc.
		l. Set SLAR RANGE DELAY switch to 40.	*l.* Measure dc voltage between J4–F and TEST POINT 5D.	*l.* +24 to +30 Vdc.
		m. Set SLAR RANGE DELAY switch to 50.	*m.* Measure dc voltage between J4–E and TEST POINT 5D.	*m.* +24 to +30 Vdc.
		n. Set SLAR RANGE DELAY switch to 60.	*n.* Measure dc voltage between J4–D and TEST POINT 5D.	*n.* +24 to +30 Vdc.
		o. Same as step *n*	*o.* Remove voltmeter leads	*o.* N/A.
		p. Set all POWER switches to OFF	*p.* Remove all jumper wires	*p.* N/A.
32	*Multimeter TS–352 B/U:* Resistance range: Rx1000.	*a.* Same as step 31*a*	*a.* Measure resistance between TEST POINTS 10A and 10C.	*a.* 4500 to 5500 ohms.
		b. BARO ALT potentiometer fully clockwise.	*b.* Connect multimeter to measure resistance between TEST POINTS 10B and 10C.	*b.* Zero Vdc.
		c. Same as step *b*	*c.* Rotate BARO ALT potentiometer slowly to fully counterclockwise stop.	*c.* Resistance increases to approximately 500 to 5500 ohms.
		d. Same as step *b*	*d.* Rotate BARO ALT potentiometer slowly to fully clockwise stop.	*d.* Resistance decreases to 0 ohms.
		e. Same as step *b*	*e.* Remove multimeter leads	*e.* N/A.
33	*Voltmeter ME–202 B/U:* De voltage range: 500.	*a.* Set CYCLING RATE switch to INTERNAL.	*a.* N/A	*a.* N/A.
		b. Set CYCLING RATE potentiometer fully clockwise.	*b.* N/A	*b.* N/A.
		c. Set all POWER switches to ON.	*c.* N/A	*c.* N/A.
		d. Same as steps *b* and *c*	*d.* Measure dc voltage between TEST POINTS 10D (+) and 6B (−).	*d.* +95 to +125 Vdc.
		e. Same as step *b*	*e.* Rotate CYCLING RATE potentiometer slowly to fully counterclockwise position, while observing dc voltage reading.	*e.* Voltage decreases slowly to less or equal to +2 Vdc.
		f. Same as step *b*	*f.* Remove voltmeter leads	*f.* N/A.
		g. Set all POWER switches to OFF.	*g.* N/A	*g.* N/A.
34	N/A	N/A	Perform roll test procedure contained in paragraph 3–25.	Readings indicated in paragraph 3–25*c*.

35	N/A	N/A	Perform pitch test procedure contained in paragraph 3-25.	Readings indicated in paragraph 3-25*d*.
36	*a. Test Set, Control Monitor-Recording Head AN/AYM-9:* (1) Set RHA TEST SELECT switch to KA60, IR/SLAR, CDM. (2) Set RHA MODE switch to CONTINUOUS.	*a.* N/A	*a.* N/A	*a.* N/A.
	b. *b* through *f* N/A	*b.* N/A	*b.* Get cable W4 from accessory case (unit 2).	*b.* N/A.
		c. N/A	*c.* Connect W4P1 to RHA IN connector J6 on test set.	*c.* N/A.
		d. N/A	*d.* Connect W4P2 to RHA IN connector J7 on test set.	*d.* N/A.
		e. Same as step 33*b*	*e.* Connect W4P3 to J3 on CM-RH test set.	*e.* N/A.
		f. Same as step 33*c*	*f.* N/A	*f.* N/A.
	g. Set OFF/ON switch to ON.	*g.* Set DISPLAY SELECT switch to KA60-1.	*g.* Observe DISPLAY CRT	*g.* CRT displays a slowly rotating circle.
	h. *h* through *k* N/A	*h.* Set DISPLAY SELECT switch to KA60-2.	*h.* Observe DISPLAY CRT	*h.* CRT displays a slowly rotating circle.
		i. Set DISPLAY SELECT switch to SLAR.	*i.* Observe DISPLAY CRT	*i.* CRT displays a slowly rotating circle.
		j. Set DISPLAY SELECT switch to KA76.	*j.* Observe DISPLAY CRT	*j.* CRT displays a slowly rotating circle.
		k. Set DISPLAY SELECT switch to CDM.	*k.* Observe DISPLAY CRT	*k.* CRT displays a slowly rotating circle.
	l. Set OFF/ON switch to OFF.	*l.* Set all POWER switches to OFF	*l.* Remove connections to test equipment.	*l.* N/A.

3-25. Pitch and Roll Test Procedures

This procedure checks out the operation of the pitch and roll sensor simulators in the test set.

a. Test Equipment Required:

(1) **Voltmeter ME-202B/U.**

(2) Ratio Transformer TF-515/V.

b. Initial Test Setup (fig. 3-37) **Make the following connections between the test equipment and the test set.**

(1) Connect the 0 terminal of the ratio transformer to the ME-202B/U.

(2) Connect the I terminal of the ratio transformer to TEST POINT 8B on the test set.

(3) Connect the C terminal of the ratio transformer to TEST POINT 8C on the test set.

(4) Connect ME-2028/U return to TEST POINT 8A.

c. Roll Test. The object of this test is to check the output of roll sensor simulator circuit as the ROLL switch is set to each of its positions, one at a time. To do this, adjust the decades on the ratio transformer until a null (zero voltage) indication is obtained on the ME-202B/U for each position of the ROLL switch. The readings you obtain must match those tabulated in the list that follows.

(1) Set all POWER switches to ON.

(2) Set the ROLL switch to the positions indicated and obtain the following readings:

ROLL switch setting	*At null, ratio transformer decades read*
-30"	0.499 to 0.501
	0.423 to 0.42s
1::	*0.34% to 0.348*
-16' I-:. mm	*0.267 to 0.269*
-10"	0.184 to 0.186
-5'	0.096 to 0.097

(3) Set all POWER switches to OFF.

(4) Remove ME-202B/U return from TEST POINT 8A and reconnect to TEST POINT 8C.

(5) Remove connection at TEST POINT 8C (from C terminal of ratio transformer) and reconnect to TEST POINT 8A.

(6) Set all POWER switches to ON.

('7) Set the ROLL switch to the positions indicated and obtain the following readings:

ROLL switch setting	*At null, ratio transformer decades read*
0°	0.000 to 0.001
5°	0.095 to 0.097
10°	0.184 to 0.186
15°	0.267 to 0.269
20°	0.346 to 0.348
25°	0.423 to 0.425
30°	0.499 to 0.501

(8) Set all POWER switches to OFF, and proceed to pitch test (*d* below).

d. *Pitch Test.* The object of this test is the same as that of the roll test (c above) except that it works to check out the pitch sensor simulators. Do not start this test until you have completed the roll test.

(1) Remove the connection at TEST POINT 8B (from the I terminal of the ratio transformer) and reconnect to TEST POINT 'ID.

(2) Remove the connection at TEST POINT 8A (from the C terminal of the ratio transformer) and reconnect to TEST POINT 8D.

(3) Connect the ME=202B/U to the 0 terminal of the ratio transformer.

(4) Connect the probe return lead to TEST POINT ?C.

(5) Set all POWER switches to ON.

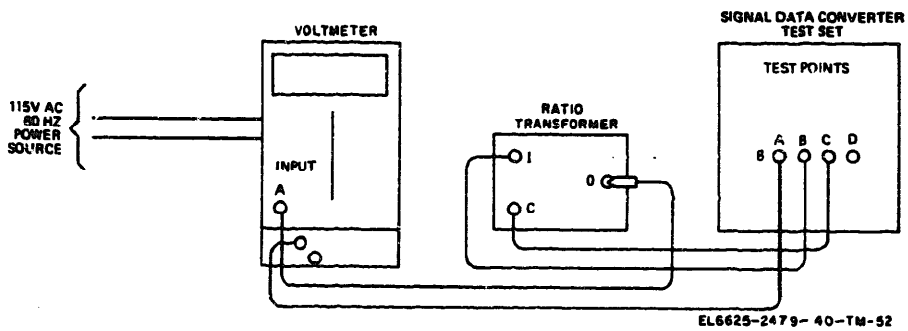

Figure 3-37. ***Roll* and *pitch test setup.***

(6) Set the PITCH switch to the positions indicated and obtain the following readings :

PITCH switch setting	*At null, ratio transformer decades read*
−9°	0.167 to 0.169
−7°	0.131 to 0.133
−5°	0.095 to 0.097
−3°	0.058 to 0.060
−2°	0.039 to 0.041
−1°	0.019 to 0.021

(7) Set all POWER switches to OFF.

(8) Remove ME-202B/U return lead from TEST POINT 9C and reconnect to TEST POINT 8D.

(9) Remove connection at TEST POINT 8D (from ratio transformer C terminal) and reconnect to TEST POINT 7C.

(10) Set all POWER switches to ON.

(11) Set the PITCH switch to the positions indicated and obtain the following readings:

PITCH switch setting	*At null, ratio transformer decades read*
0	0.000 to 0.001
1	0.019 to 0.021
2	0.039 to 0.041
3	0.058 to 0.060
5	0.095 to 0.097
7	0.131 to 0.133
9	0.167 to 0.169

(12) Set all POWER switches to OFF.

(13) Remove all test connections.

APPENDIX A

REFERENCES

The following publications contain information applicable to general support maintenance of Test Set, Signal Data Converter AN/AYM-8.

DA Pam 310-4	Index of Technical Manuals, Technical Bulletins, Supply Manuals (types 7, 8, and 9), Supply Bulletins, and Lubrication Orders
DA Pam 316-7	U.S. Army Equipment Index of Modification Work Orders
TM 11-6625366-15	Operator's, Organizational, DS, GS, and Depot Maintenance Manual : Multimeter TS352B/U
TM 11-6625-537-15-l	Organizational, DS, GS, and Depot Maintenance Manual : Voltmeter, Electronic ME-202A/U
TM 11-6625-1703-15	Operator, Organizational, DS, GS, and Depot Maintenance ing Repair Parts and Special Tool Lists: Oscilloscope
TM 11-6625-247~12	Operator's Organizational Maintenance Manual, Includin and Speciai Tools List: Test Set, Control Monitor-Recording Head AN/AYM-9 (FSN 6625-150-1882)
TM 11-6625-2479-12	Operator's and Organizational Maintenance Manual, Including Repair Parts and Special Tools List: Test Set, Signal Data Converter AN/AYM-8 (FSN 6625-W-2289)
TM 38-750	The Army Maintenance Management System (TAMMS)

GLOSSARY

Abbreviation	De~tiorr
ADAS	**Airborne Data Annotation System AN/AYA-10**
ALT	**Alternate**
Alt	**Altitude**
Baro Alt	**Barometric Altitude Analog**
BCD	**Binary coded decimal**
CDM	**Control-Monitor G8338/AYA-10**
CM-RH test set	**Test Set, Control Monitor-Recording Head AN/AYM-9**
CRT	**Cathode ray tube**
INS	**Inertial navigation system**
IR	**Detecting Set, Infrared AN/AAS-24**
KA60–1	**Forward Panoramic Camera Surveillance System KA-GOC**
KA60–2	**Aft Vertical Panoramic Camera Survelliance System KA-60C**
KA–76	**Airborne Photographic Surveillance System KS-113A**
kHz	**Kilohertz**
NUM	**Numeric**
SLAR	**Radar Surveillance Set AN/APS-941)**
SDC	**Converter, Signal Data CV-2647/AYA-10**
SDC test set	**Test Set, Signal Data Converter AN/AYM-8**
Vg/H	**Ratio of aircraft ground velocity to altitude**

INDEX

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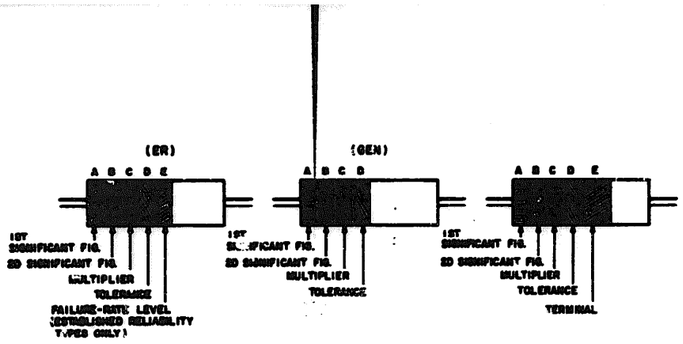


COLOR CODE MARKING FOR COMPOSITION TYPE RESISTORS.

COLOR-CODE MARKING FOR FILM-TYPE RESISTORS.

TABLE I
COLOR CODE FOR COMPOSITION TYPE AND FILM TYPE RESISTORS.

BAND A		BAND B		BAND C		BAND D		BAND E		
COLOR	FIRST SIGNIFICANT FIGURE	COLOR	SECOND SIGNIFICANT FIGURE	COLOR	MULTIPLIER	COLOR	RESISTANCE TOLERANCE (PERCENT)	COLOR	FAILURE RATE LEVEL	TERM.
BLACK	0	BLACK	0	BLACK	1			BROWN	M=1.0	
BROWN	1	BROWN	1	BROWN	10			RED	P=0.1	
RED	2	RED	2	RED	100			ORANGE	R=0.01	
ORANGE	3	ORANGE	3	ORANGE	1,000			YELLOW	S=0.001	
YELLOW	4	YELLOW	4	YELLOW	10,000	SILVER	±10 (COMP. TYPE ONLY)	WHITE		SOLDERABLE
GREEN	5	GREEN	5	GREEN	100,000	GOLD	±5			
BLUE	6	BLUE	6	BLUE	1,000,000	RED	±2 (NOT APPLICABLE TO ESTABLISHED RELIABILITY).			
PURPLE (VIOLET)	7	PURPLE (VIOLET)	7							
GRAY	8	GRAY	8	SILVER	0.01					
WHITE	9	WHITE	9	GOLD	0.1					

BAND A — THE FIRST SIGNIFICANT FIGURE OF THE RESISTANCE VALUE (BANDS A THRU D SHALL BE OF EQUAL WIDTH.)

BAND B — THE SECOND SIGNIFICANT FIGURE OF THE RESISTANCE VALUE.

BAND C — THE MULTIPLIER (THE MULTIPLIER IS THE FACTOR BY WHICH THE TWO SIGNIFICANT FIGURES ARE MULTIPLIED TO YIELD THE NOMINAL RESISTANCE VALUE.)

BAND D — THE RESISTANCE TOLERANCE.

BAND E — WHEN USED ON COMPOSITION RESISTORS, BAND E INDICATES ESTABLISHED RELIABILITY FAILURE-RATE LEVEL (PERCENT FAILURE PER 1,000 HOURS). ON FILM RESISTORS, THIS BAND SHALL BE APPROXIMATELY 1-1/2 TIMES THE WIDTH OF OTHER BANDS, AND INDICATES TYPE OF TERMINAL.

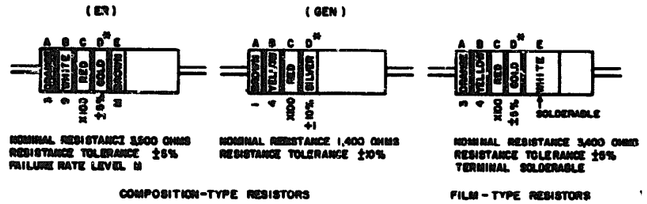
RESISTANCES IDENTIFIED BY NUMBERS AND LETTERS (THESE ARE NOT COLOR CODED)

SOME RESISTORS ARE IDENTIFIED BY THREE OR FOUR DIGIT ALPHA NUMERIC DESIGNATORS. THE LETTER R IS USED IN PLACE OF A DECIMAL POINT WHEN FRACTIONAL VALUES OF AN OHMS ARE EXPRESSED. FOR EXAMPLE:

2R7 = 2.7 OHMS 10R0 = 10.0 OHMS

FOR WIRE-WOUND-TYPE RESISTORS COLOR CODING IS NOT USED, IDENTIFICATION MARKING IS SPECIFIED IN EACH OF THE APPLICABLE SPECIFICATIONS.

EXAMPLES OF COLOR CODING



NOMINAL RESISTANCE 1,500 OHMS
RESISTANCE TOLERANCE ±5%
FAILURE RATE LEVEL M

NOMINAL RESISTANCE 1,400 OHMS
RESISTANCE TOLERANCE ±10%

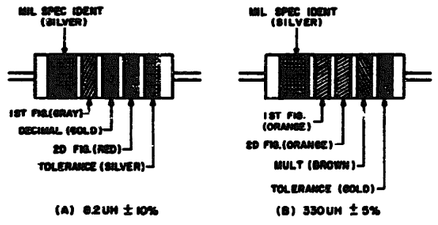
NOMINAL RESISTANCE 3,400 OHMS
RESISTANCE TOLERANCE ±5%
TERMINAL SOLDERABLE

COMPOSITION-TYPE RESISTORS

FILM-TYPE RESISTORS

* IF BAND D IS OMITTED, THE RESISTOR TOLERANCE IS ±20% AND THE RESISTOR IS NOT MIL-STD.

A. COLOR CODE MARKING FOR MILITARY STANDARD RESISTORS.



(A) 0.2UH ± 10%

(B) 330UH ± 5%

COLOR CODING FOR TUBULAR ENCAPSULATED R.F. CHOKES. AT A, AN EXAMPLE OF OF THE CODING FOR AN 0.2UH CHOKE IS GIVEN. AT B, THE COLOR BANDS FOR A 330UH INDUCTOR ARE ILLUSTRATED.

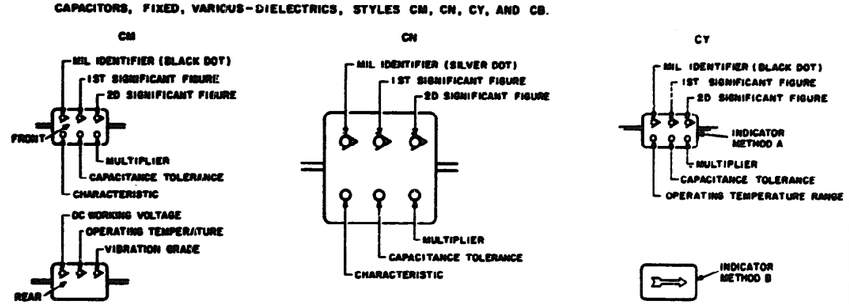
TABLE 2
COLOR CODING FOR TUBULAR ENCAPSULATED R.F. CHOKES.

COLOR	SIGNIFICANT FIGURE	MULTIPLIER	INDUCTANCE TOLERANCE (PERCENT)
BLACK	0	1	
BROWN	1	10	1
RED	2	100	2
ORANGE	3	1,000	3
YELLOW	4		
GREEN	5		
BLUE	6		
VIOLET	7		
GRAY	8		
WHITE	9		
NONE			20
SILVER			10
GOLD	DECIMAL POINT		5

MULTIPLIER IS THE FACTOR BY WHICH THE TWO COLOR FIGURES ARE MULTIPLIED TO OBTAIN THE INDUCTANCE VALUE OF THE CHOKE COIL.

B. COLOR CODE MARKING FOR MILITARY STANDARD INDUCTORS.

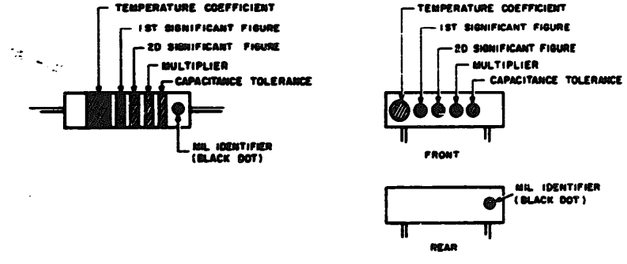
CAPACITORS, FIXED, VARIOUS-DIELECTRICS, STYLES CM, CN, CY, AND CB.



MICA-DIELECTRIC

PAPER-DIELECTRIC

GLASS-DIELECTRIC, GLASS CASE

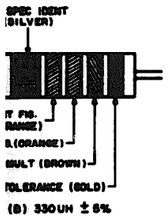


AXIAL LEAD

RADIAL LEAD

C. COLOR CODE

Figure FO-1 Color codes for military standard resistors, inductors, and capacitors.



CHOKES. AT A, AN EXAMPLE OF
. AT B, THE COLOR BANDS FOR

MPSULATED R.F. CHOKES.

	INDUCTANCE TOLERANCE (PERCENT)
	1
	2
	3
	20
	10
	5

N THE TWO COLOR FIGURES
CTANCE VALUE OF THE

IV STANDARD INDUCTORS.

CAPACITORS, FIXED, VARIOUS-DIELECTRICS, STYLES CM, CN, CY, AND CB.

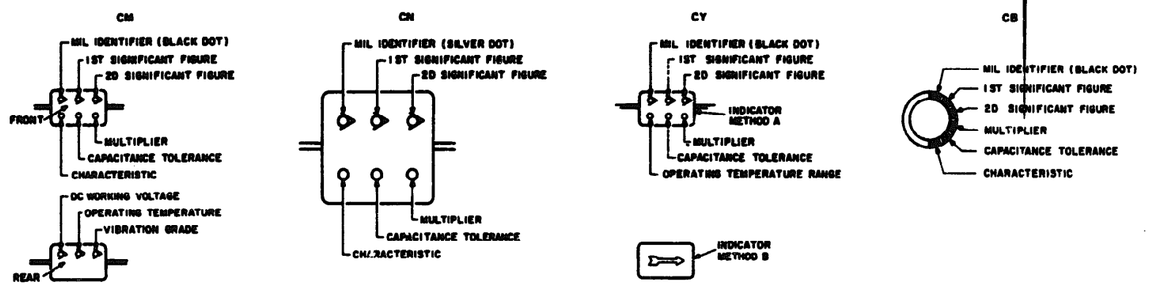


TABLE 3 — FOR USE WITH STYLES CM, CN, CY AND CB.

COLOR	MIL ID	1ST SIG FIG.	2D SIG FIG.	MULTIPLIER[1]	CAPACITANCE TOLERANCE				CHARACTERISTIC[2]			DC WORKING VOLTAGE	OPERATING TEMP. RANGE	VIBRATION GRADE
					CM	CN	CY	CB	CM	CN	CB	CN	CY, CN	CM
BLACK	CM,CY CB	0	0	1			±20%	±20%		A			-55°TO+70°C	10-55 HZ
BROWN		1	1	10					B	E	B			
RED		2	2	100	±2%		±2%	±2%	C				-55°TO+85°C	
ORANGE		3	3	1,000		±30%			D		D	300		
YELLOW		4	4	10,000					E				-55°TO+125°C	10-2,000HZ
GREEN		5	5		±5%				F			500		
BLUE		6	6										-55°TO+150°C	
PURPLE (VIOLET)		7	7											
GREY		8	8											
WHITE		9	9											
GOLD				0.1			±5%	±5%						
SILVER	CN				±10%	±10%	±10%	±10%						

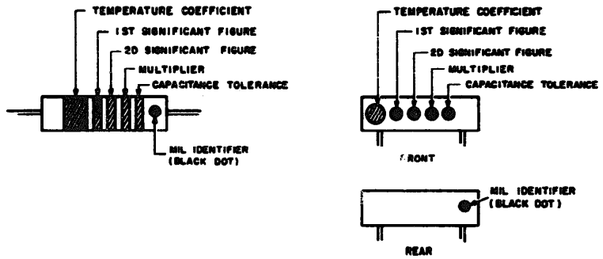


TABLE 4 — TEMPERATURE COMPENSATING, STYLE CC.

COLOR	TEMPERATURE COEFFICIENT[4]	1ST SIG FIG.	2D SIG FIG.	MULTIPLIER[1]	CAPACITANCE TOLERANCE		MIL ID
					CAPACITANCES OVER 10 UUF	CAPACITANCES 10 UUF OR LESS	
BLACK	0	0	0	1		±2.0 UUF	CC
BROWN	-30	1	1	10	±1%		
RED	-80	2	2	100	±2%	±0.25 UUF	
ORANGE	-150	3	3	1,000			
YELLOW	-220	4	4				
GREEN	-330	5	5		±5%	±0.5 UUF	
BLUE	-470	6	6				
PURPLE (VIOLET)	-750	7	7				
GREY		8	8	0.01			
WHITE		9	9	0.1	±10%		
GOLD	+100					±1.0 UUF	
SILVER							

1. THE MULTIPLIER IS THE NUMBER BY WHICH THE TWO SIGNIFICANT (SIG) FIGURES ARE MULTIPLIED TO OBTAIN THE CAPACITANCE IN UUF.
2. LETTERS INDICATE THE CHARACTERISTICS DESIGNATED IN APPLICABLE SPECIFICATIONS: MIL-C-5, MIL-C-250, MIL-C-11272B, AND MIL-C-10950C RESPECTIVELY.
3. LETTERS INDICATE THE TEMPERATURE RANGE AND VOLTAGE-TEMPERATURE LIMITS DESIGNATED IN MIL-C-11015D.
4. TEMPERATURE COEFFICIENT IN PARTS PER MILLION PER DEGREE CENTIGRADE.

C. COLOR CODE MARKING FOR MILITARY STANDARD CAPACITORS.

ESC-FM 1794-71

Figure FO-1 Color codes for military standard resistors, inductors, and capacitors.

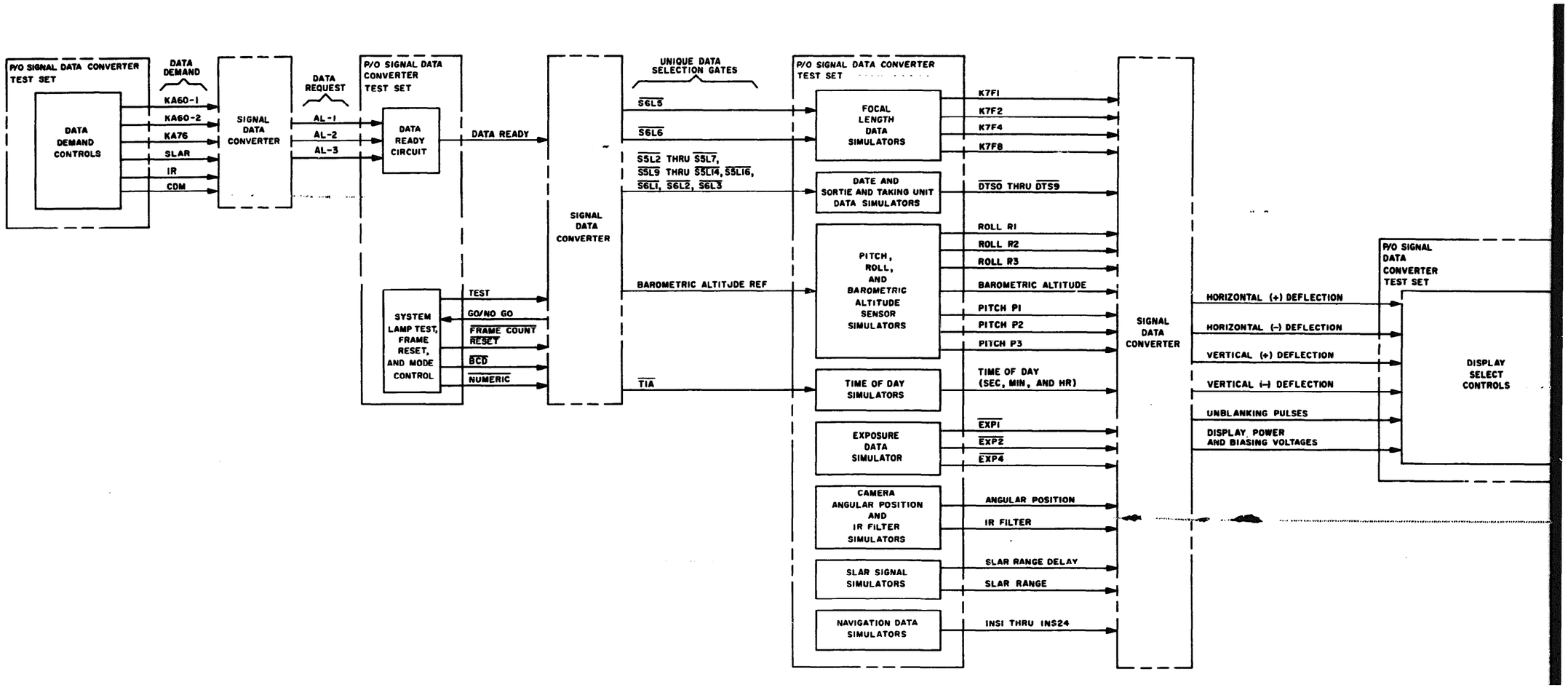


Figure FO-2. Test set, block diagram.

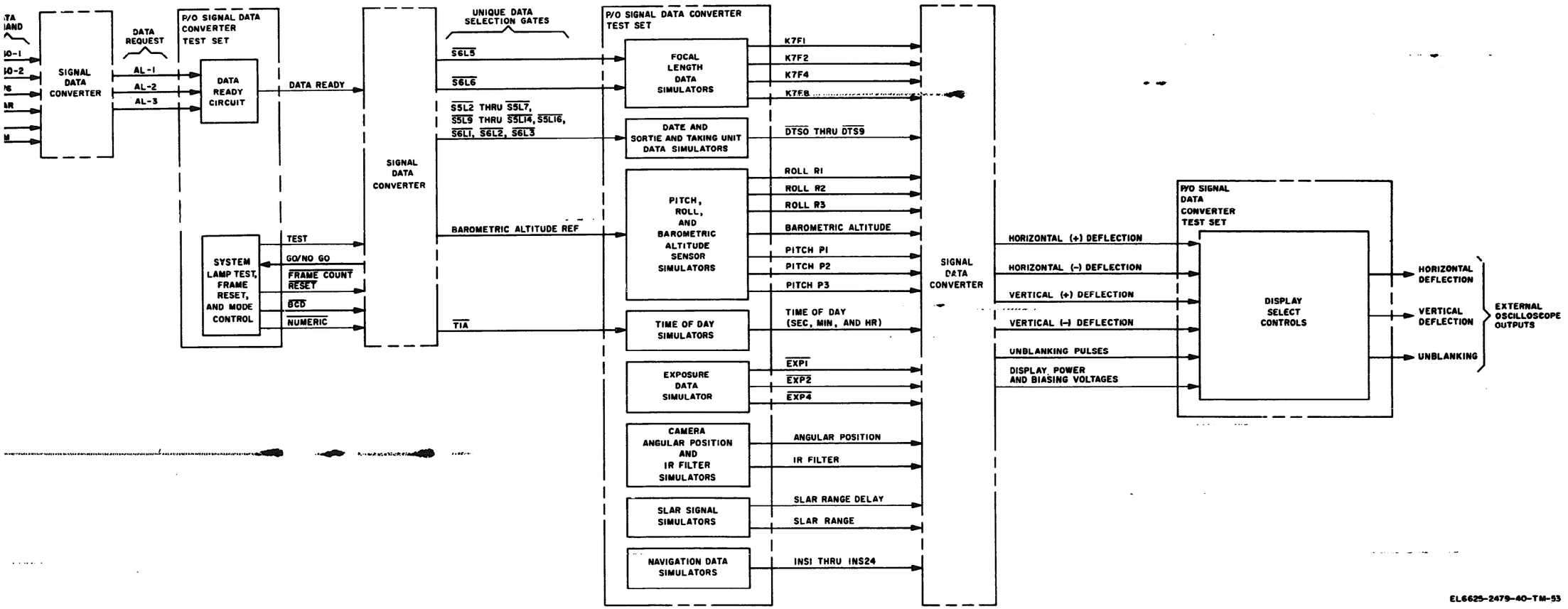


Figure FO-2. Test set, block *diagram.*

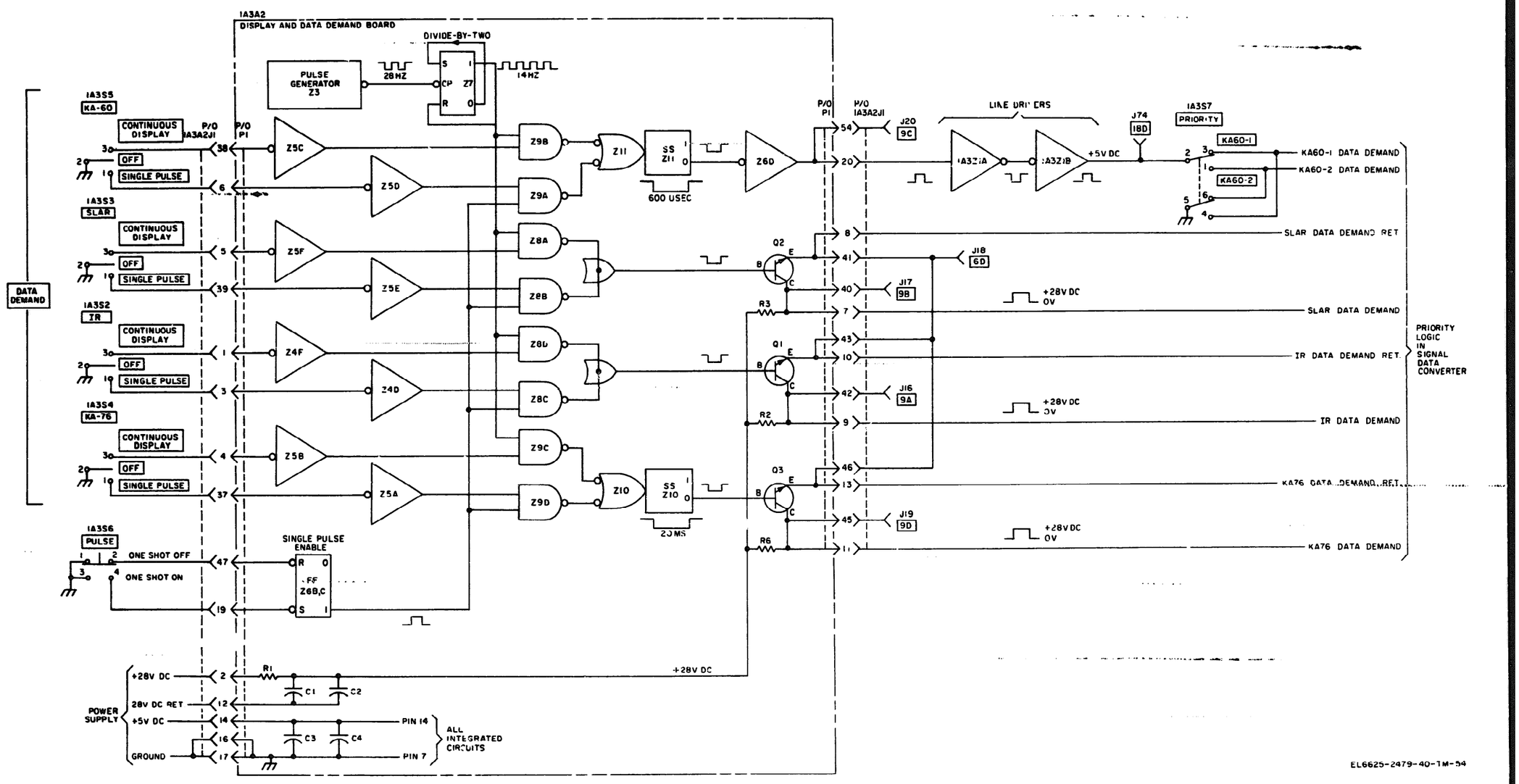


Figure FO-3. Data demand control, block diagram.

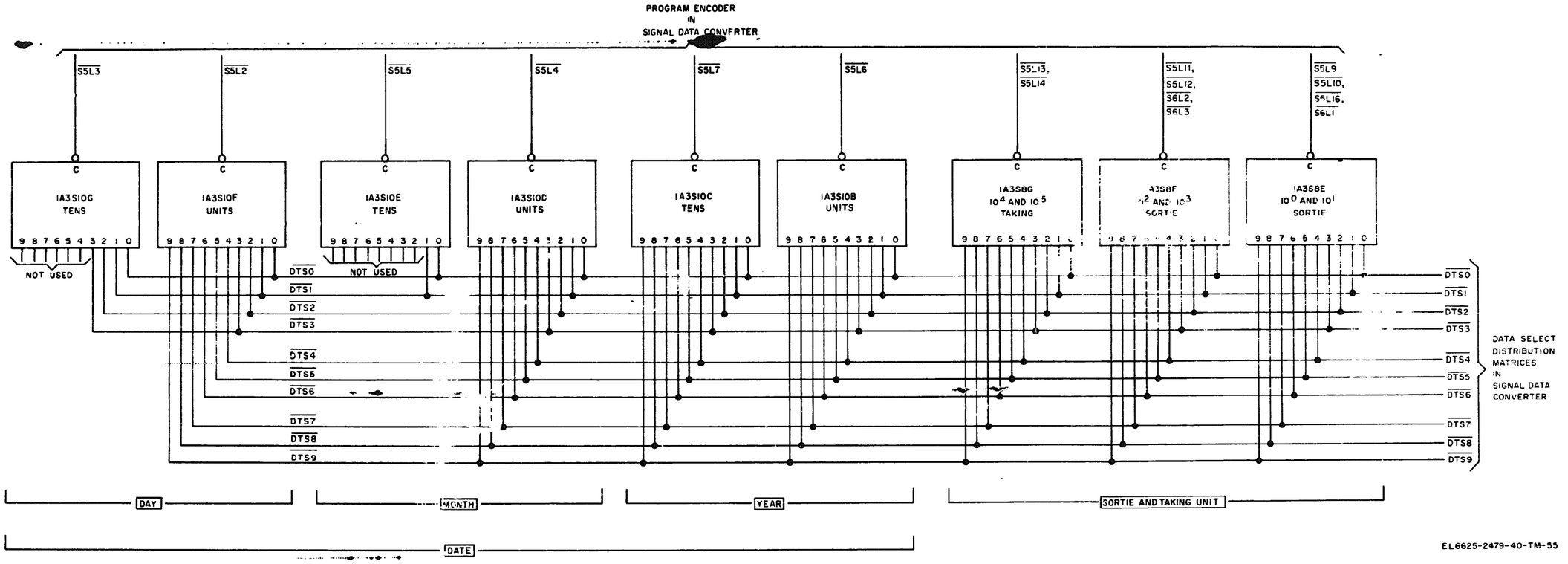


Figure FO-3_ .te, **taking** *unit, and sortie simulators, block diagram.*

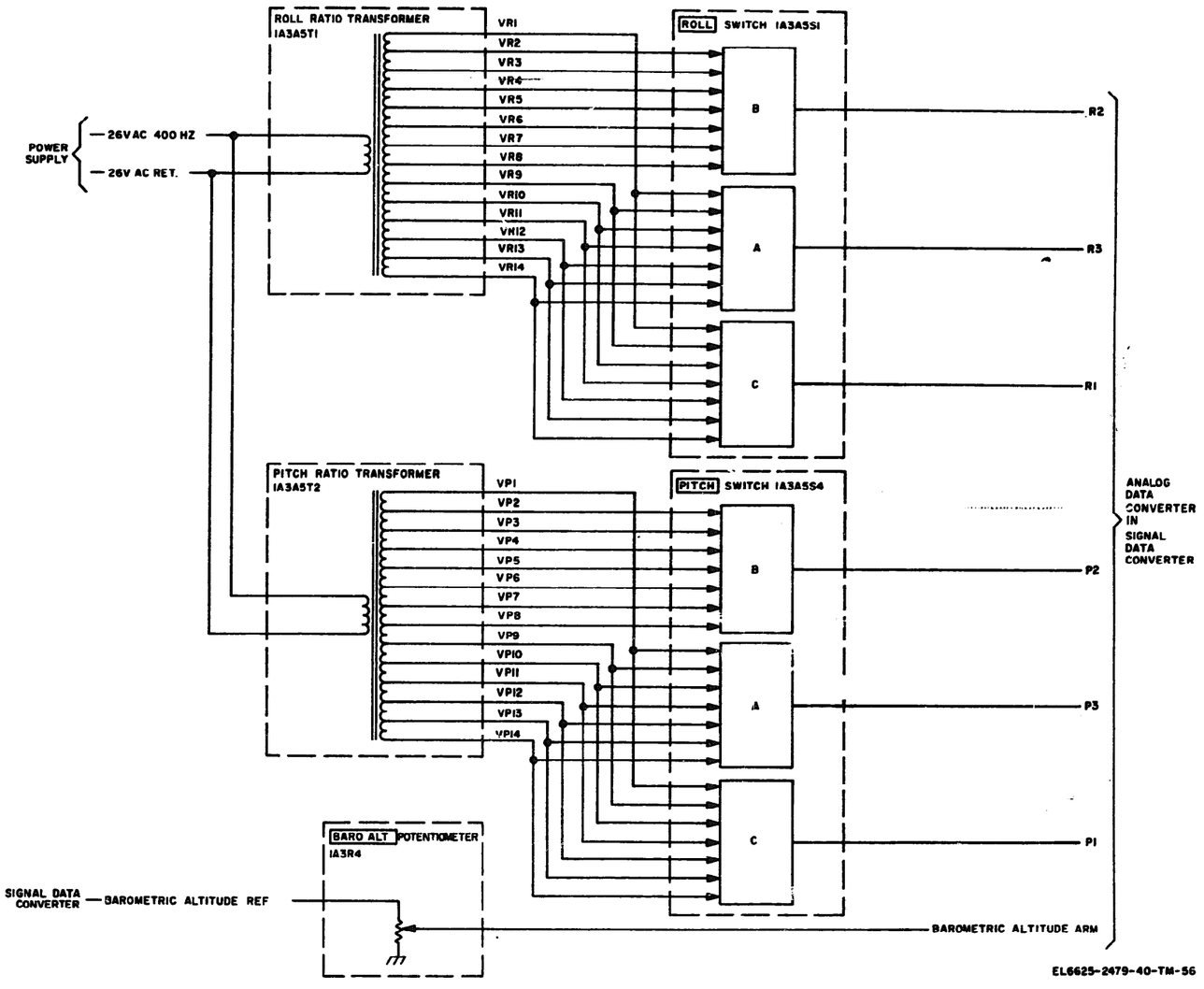


Figure FO-5. Pitch, roll, and barometric altitude simulation block diagram.

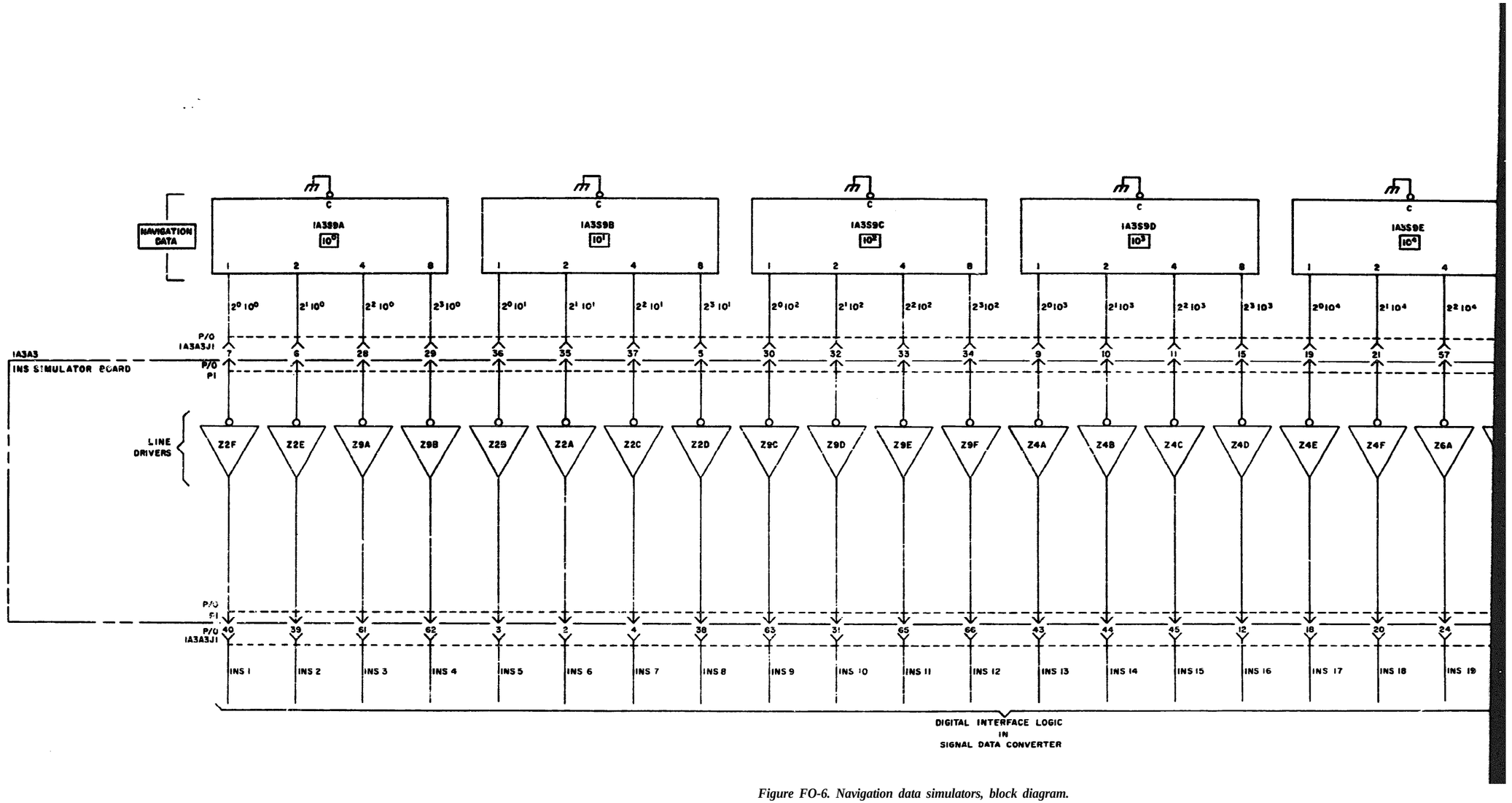


Figure FO-6. Navigation data simulators, block diagram.

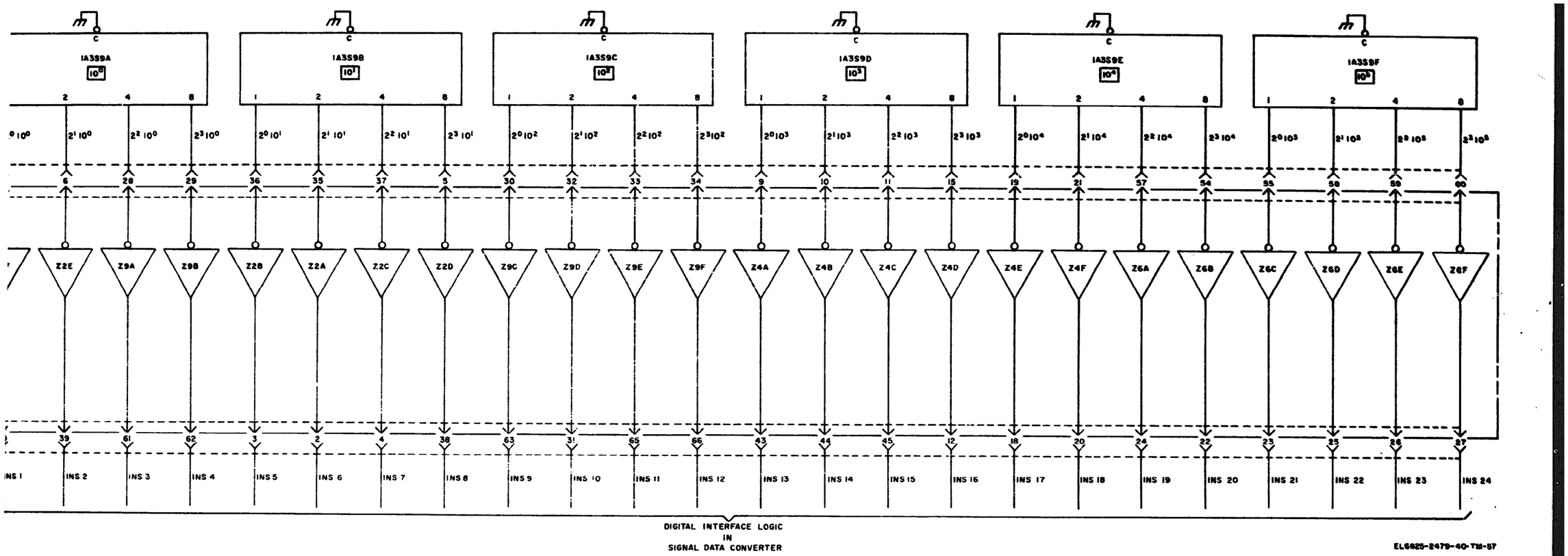


Figure FO-6. Navigation data simulators, block diagram.

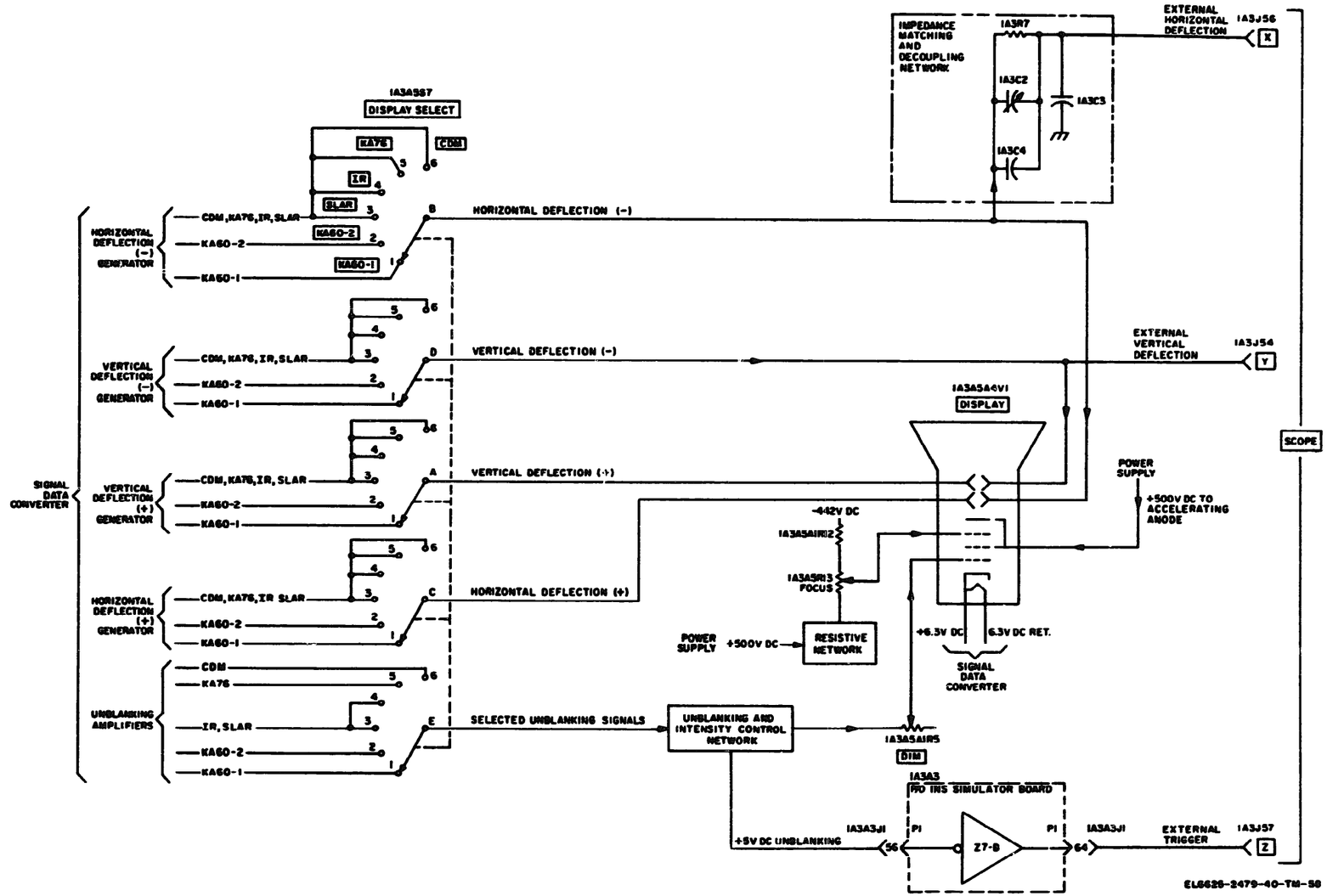


Figure FO-7. Display select controls, block diagram.

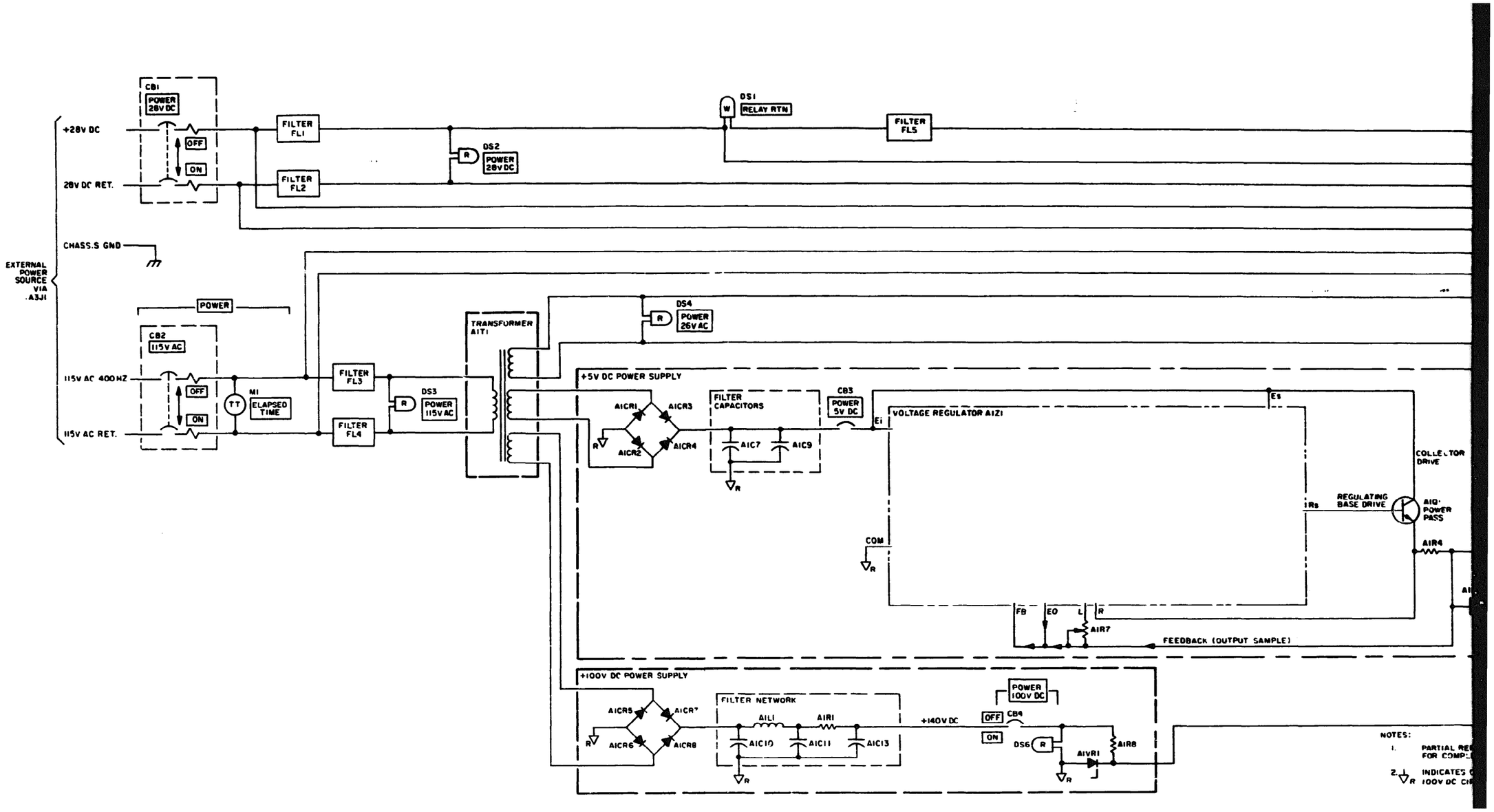


Figure FO-8 Power supply, block diagram.

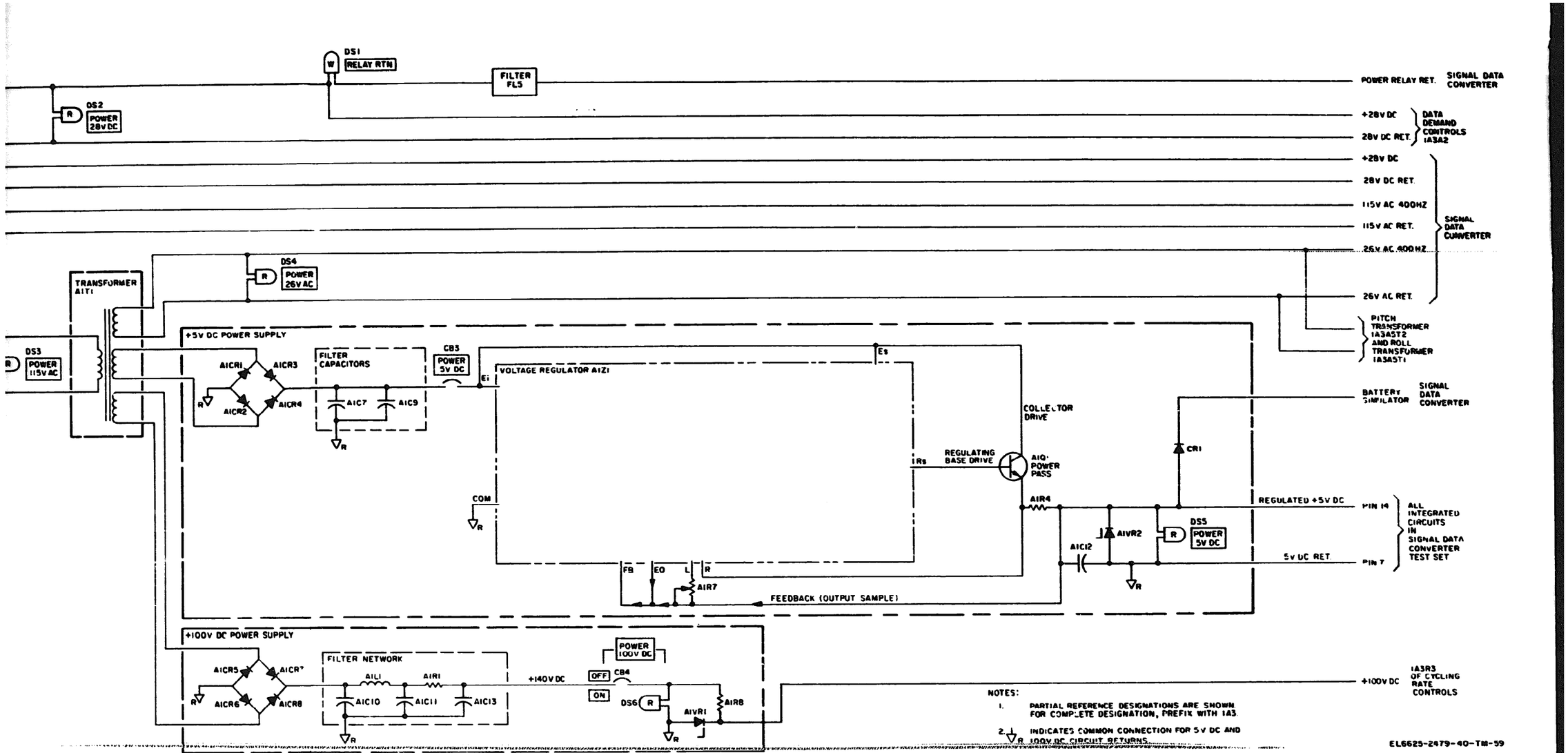


Figure FO-8. Power supply, block diagram.

NOTES:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATION, PREFIX WITH 1A3 AND SUBASSEMBLY DESIGNATIONS.
2. UNLESS OTHERWISE SPECIFIED: RESISTANCE VALUES ARE IN OHMS, 1/4W, ±5%. CAPACITANCE VALUES ARE IN MICROFARADS, ±10%, 1000V.
3. COMMON CONNECTION CIRCUIT RETURN SYMBOL IDENTIFICATIONS ARE AS FOLLOWS:
   - A: +5V DC
   - B: 5V DC RETURN
   - C: 26V AC
   - D: 26V AC RETURN
   - E: +28V DC
   - F: 28V DC RETURN
   - S: SIG SHLD GROUND
   - T: EMI SHLD GROUND
   - H: +100V DC

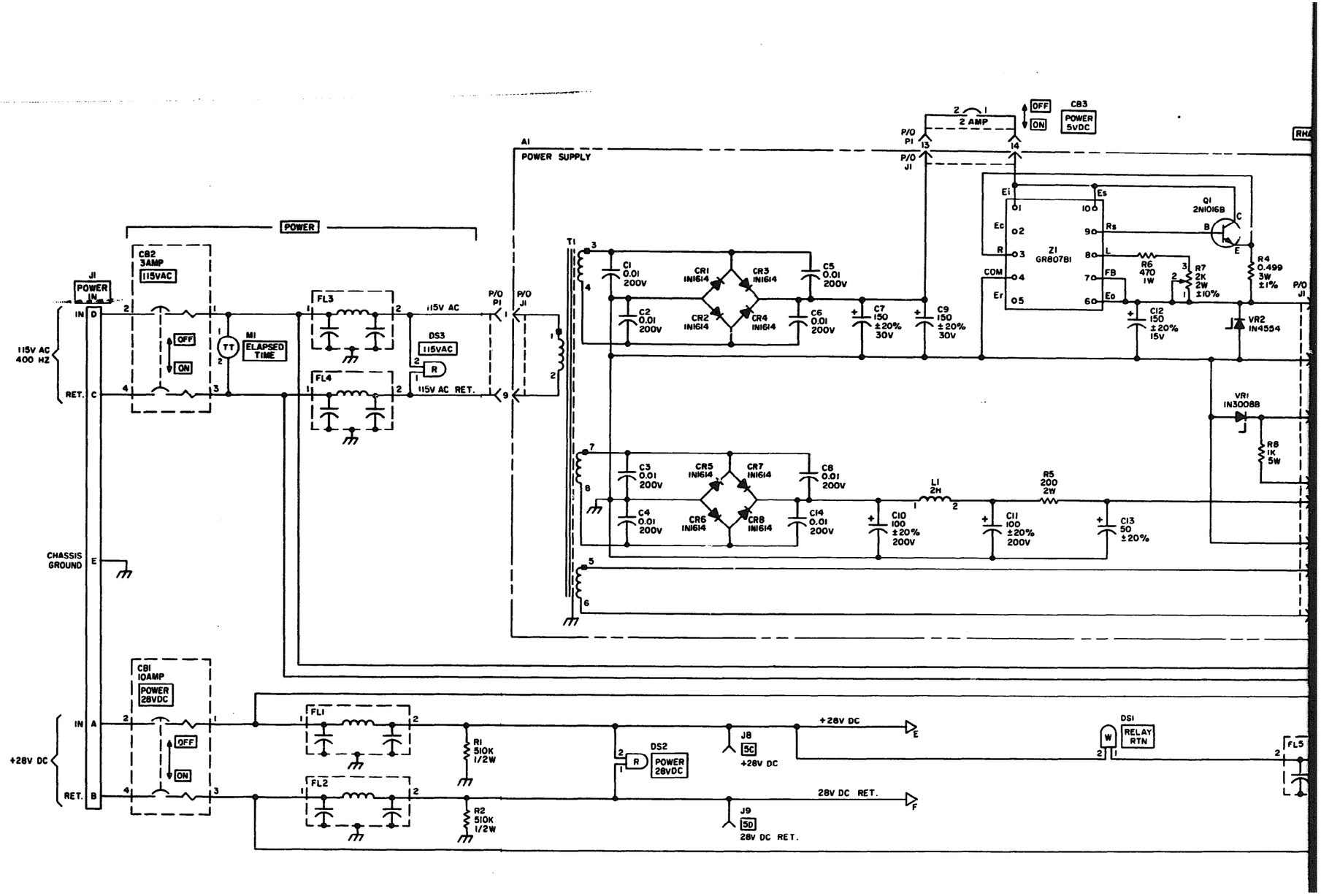


Figure FO-90. Teat set, schematic diagram (part 1 of 5).

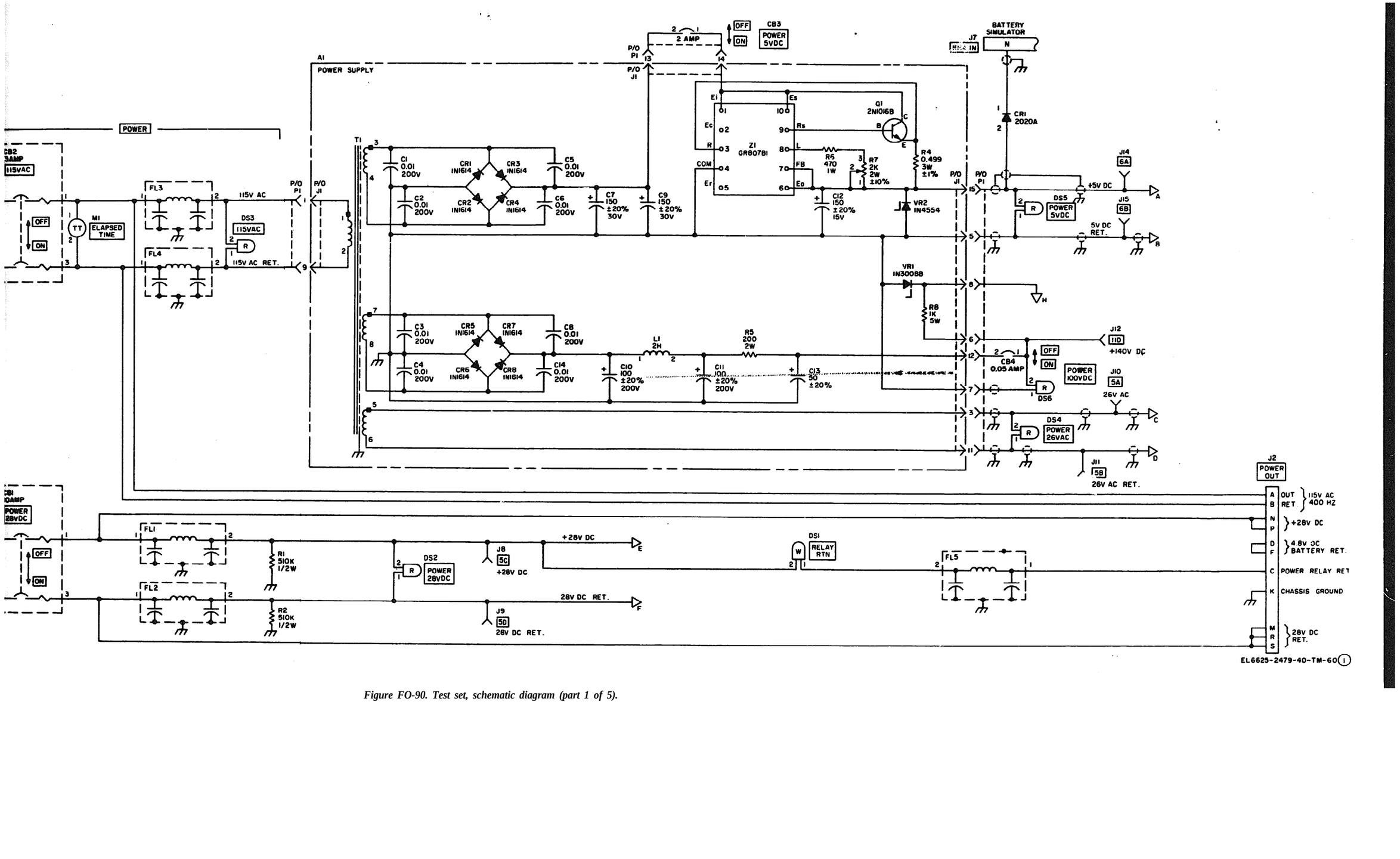


Figure FO-90. Test set, schematic diagram (part 1 of 5).

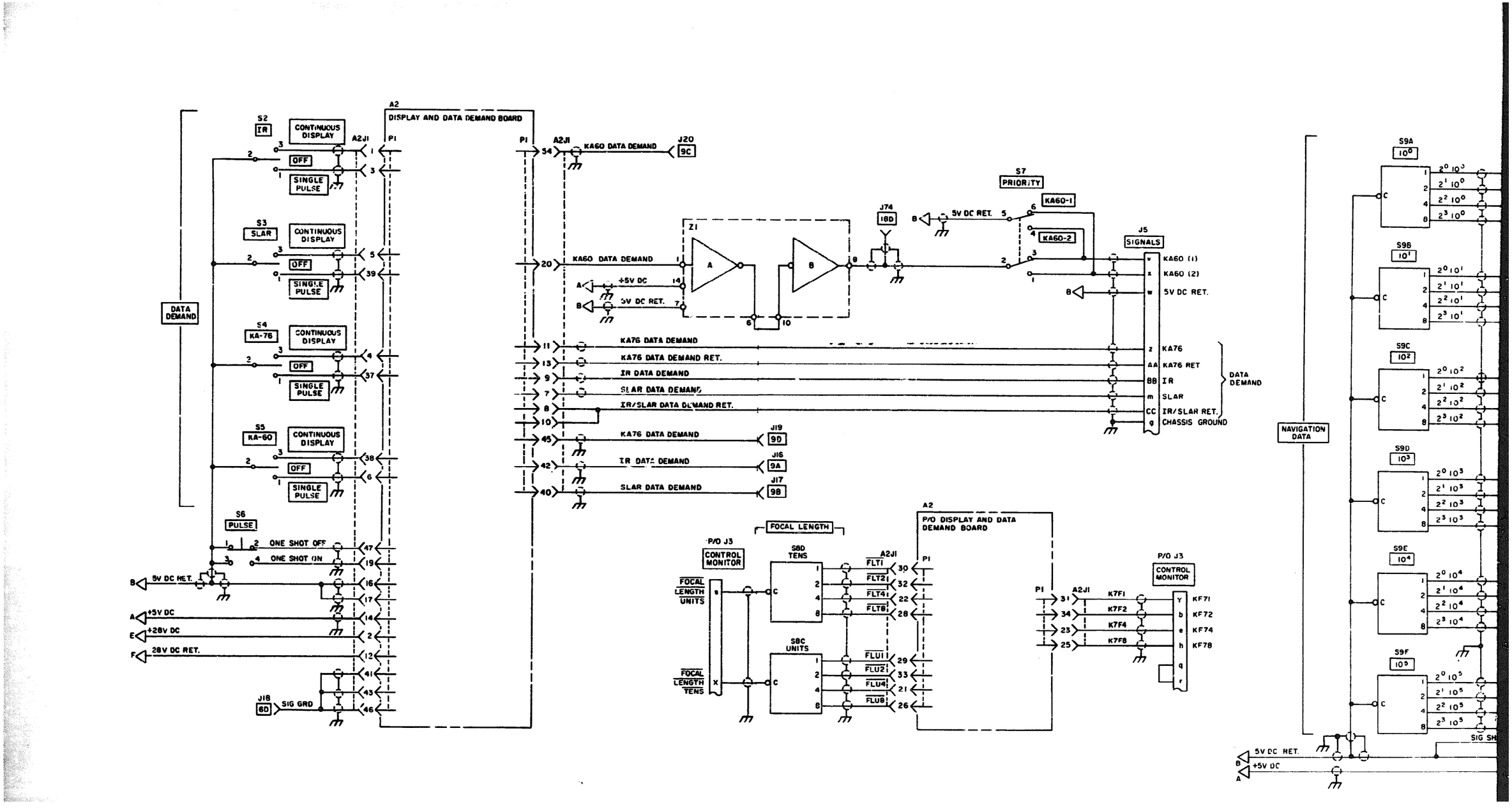


Figure *FO-90. Test set, alarm diagram (part 2 of 5).*

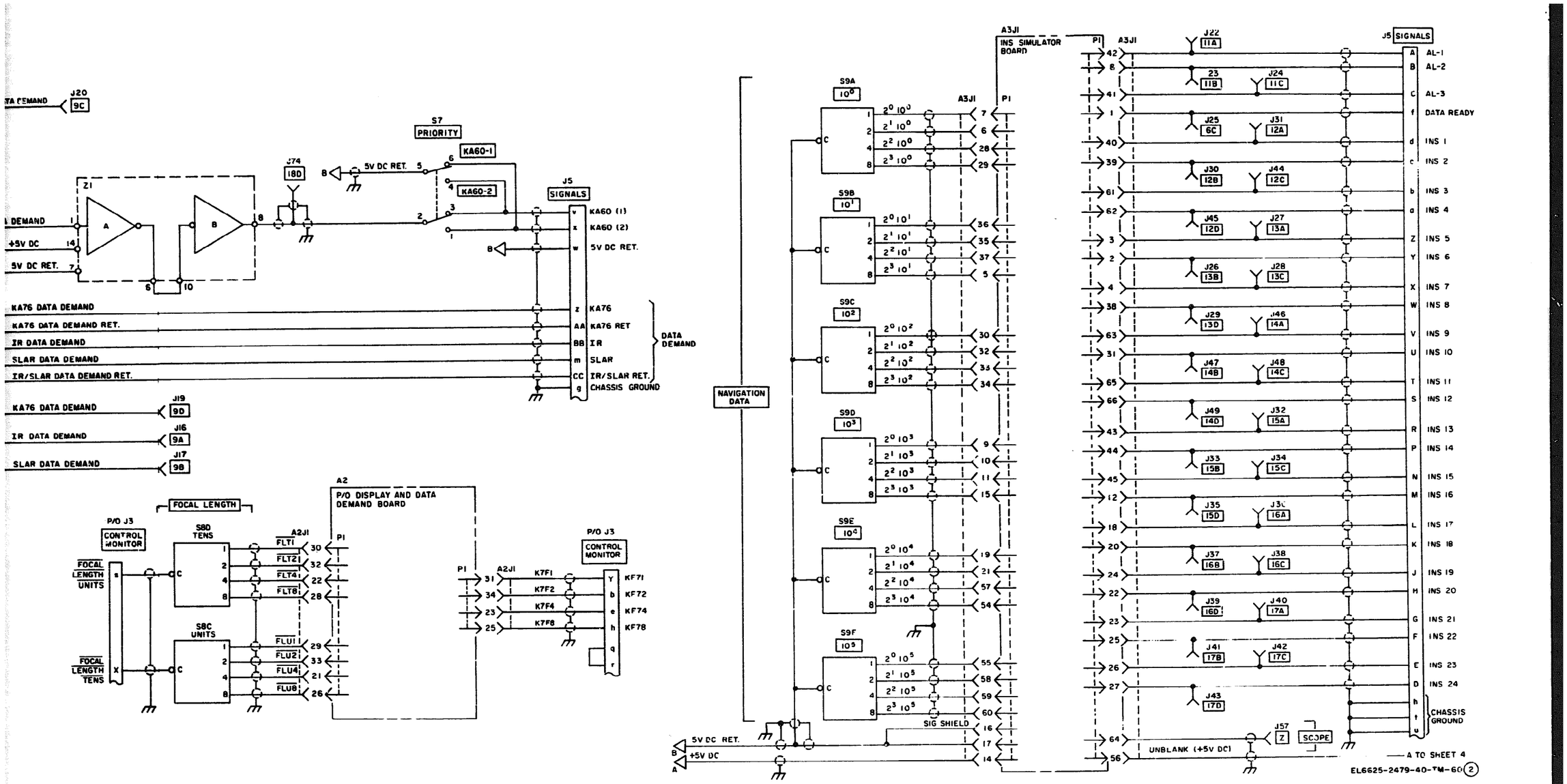


Figure FO-90. Test set, schematic diagram *(part 2 of 5).*

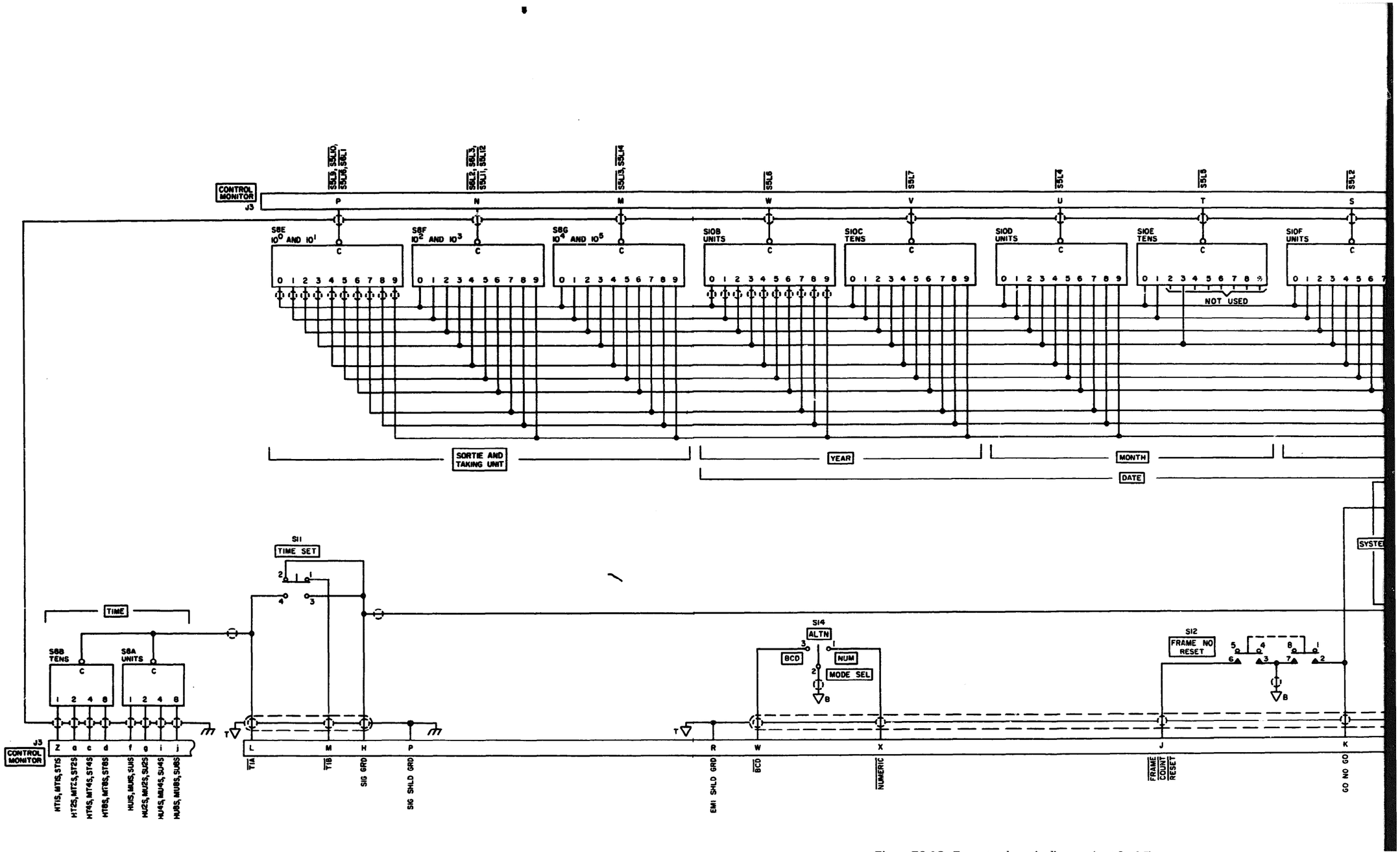


Figure FO-9@. Test set, schematic diagram (part 3 of 5).

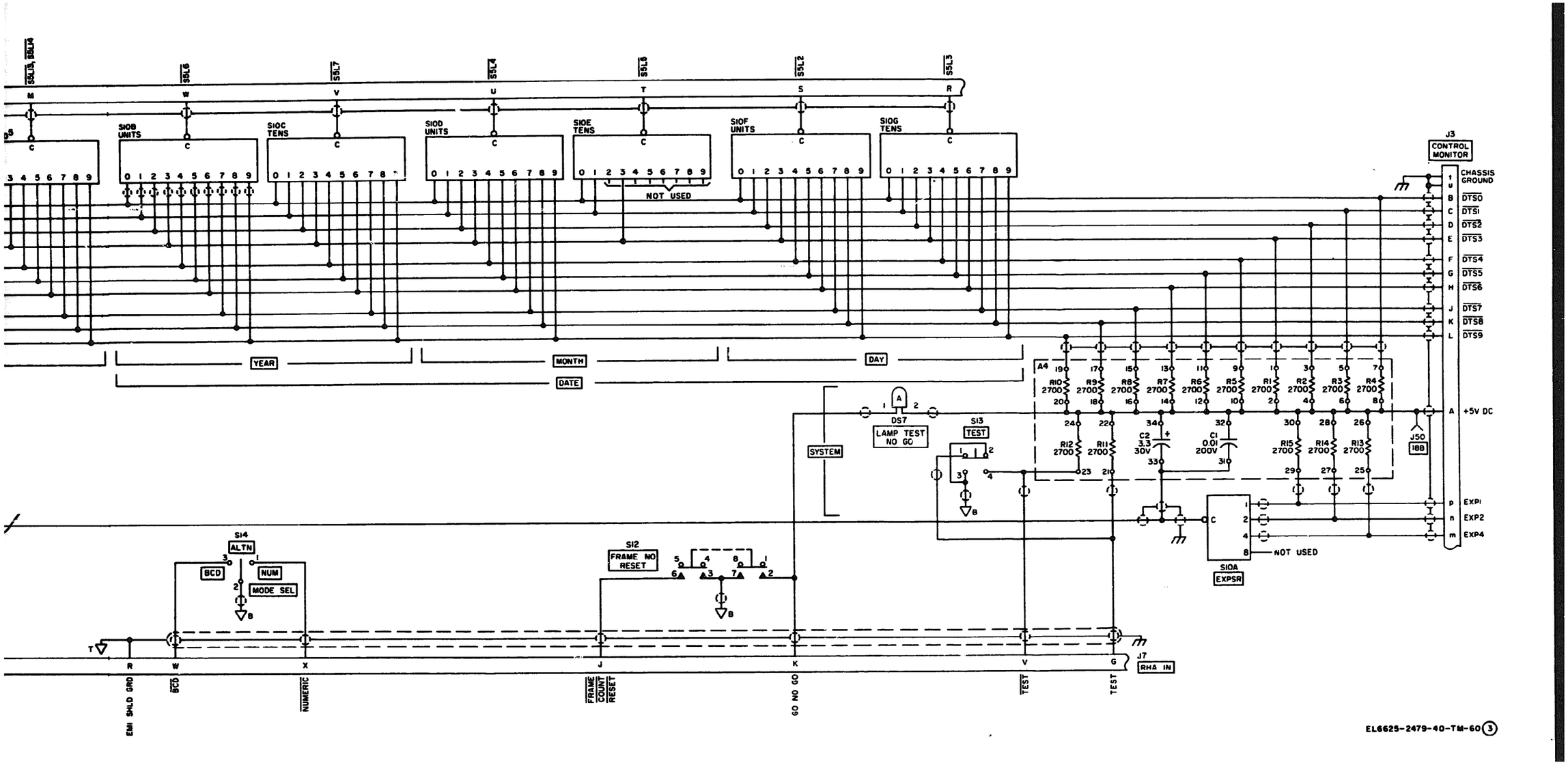


Figure FO-9@. Test set, schematic diagram (part 3 of 5).

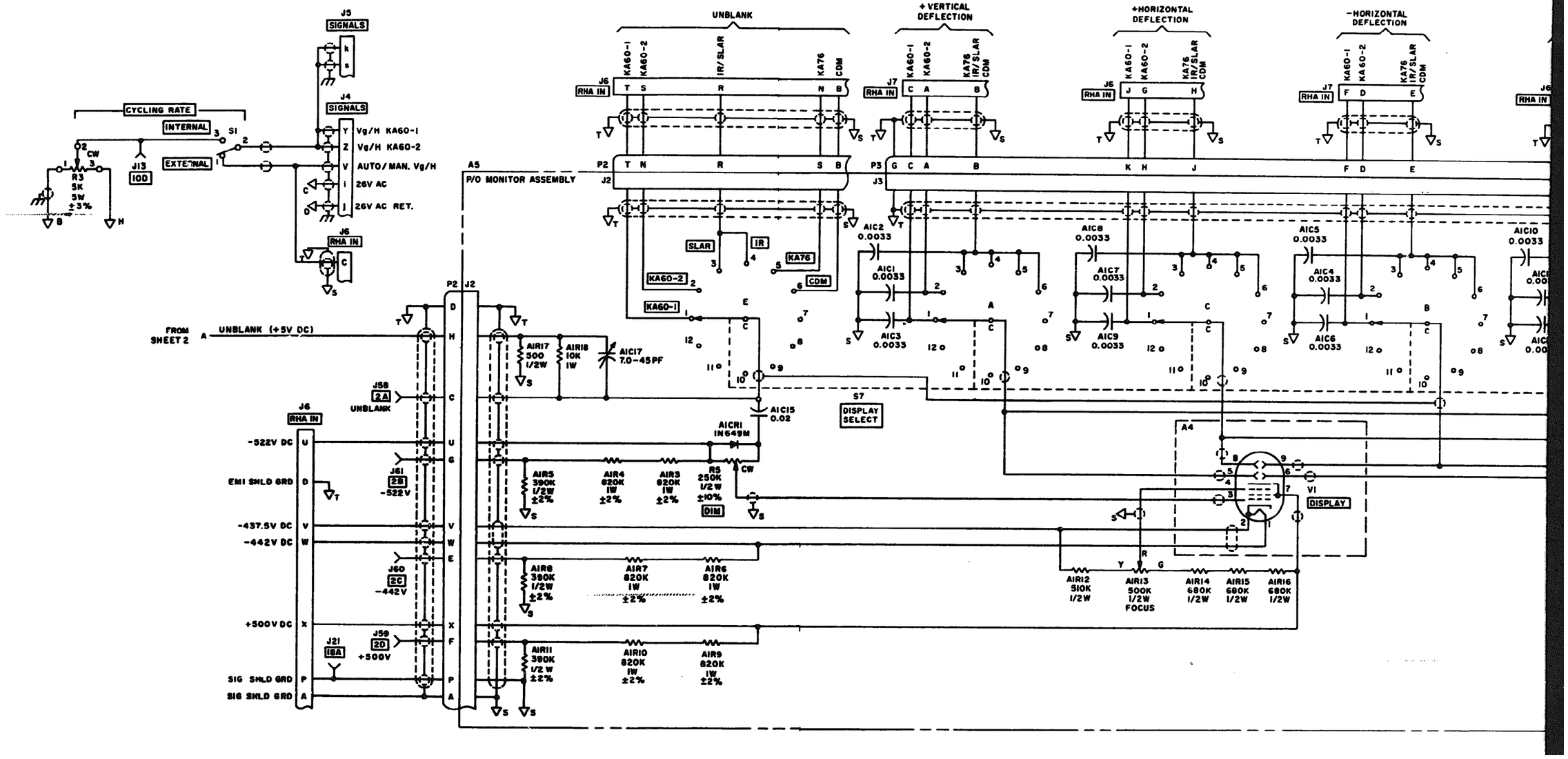


Figure FO-9@. Test set, schematic diagram (part 4 of 5).

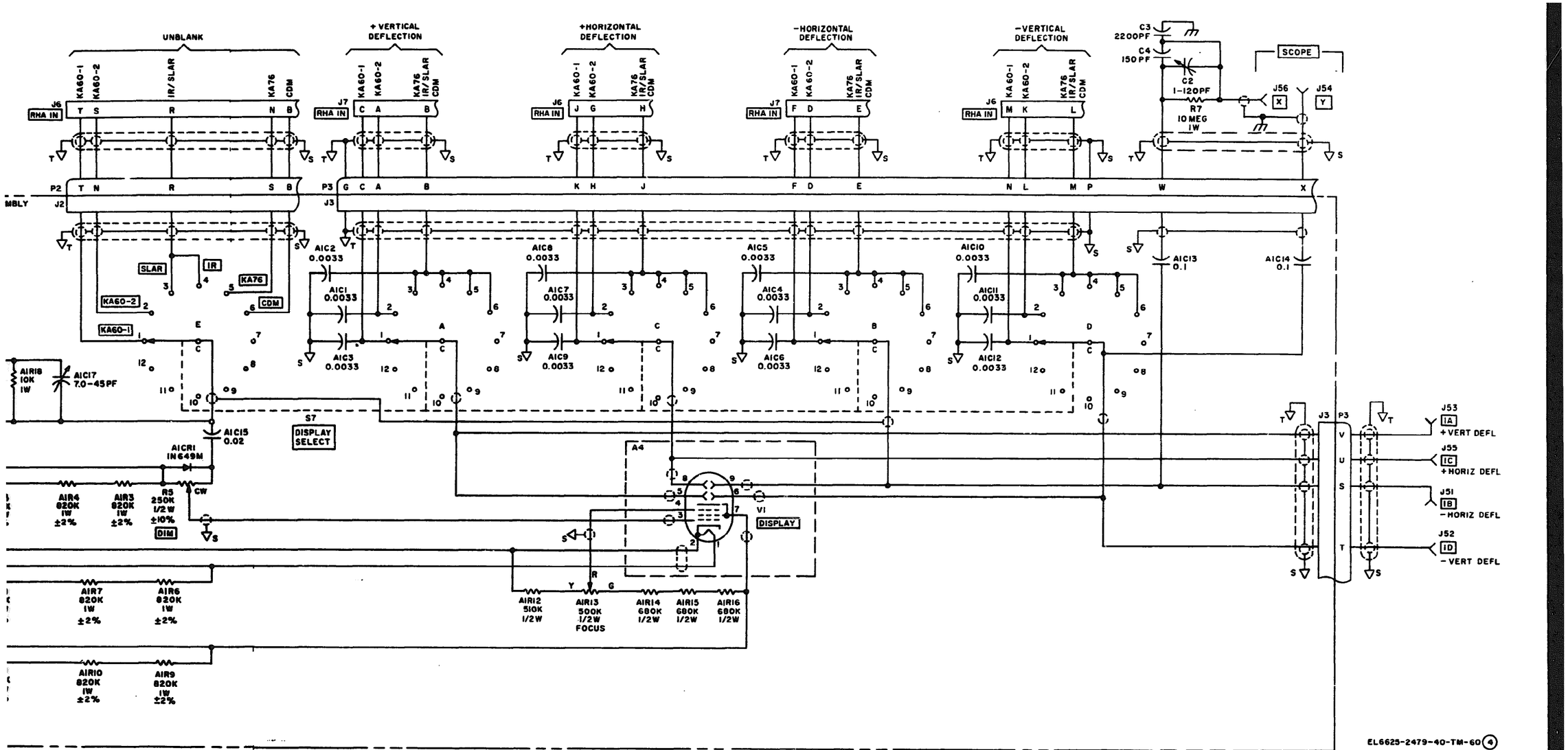


Figure FO-9. Test set, schematic diagram (part 4 of 5).

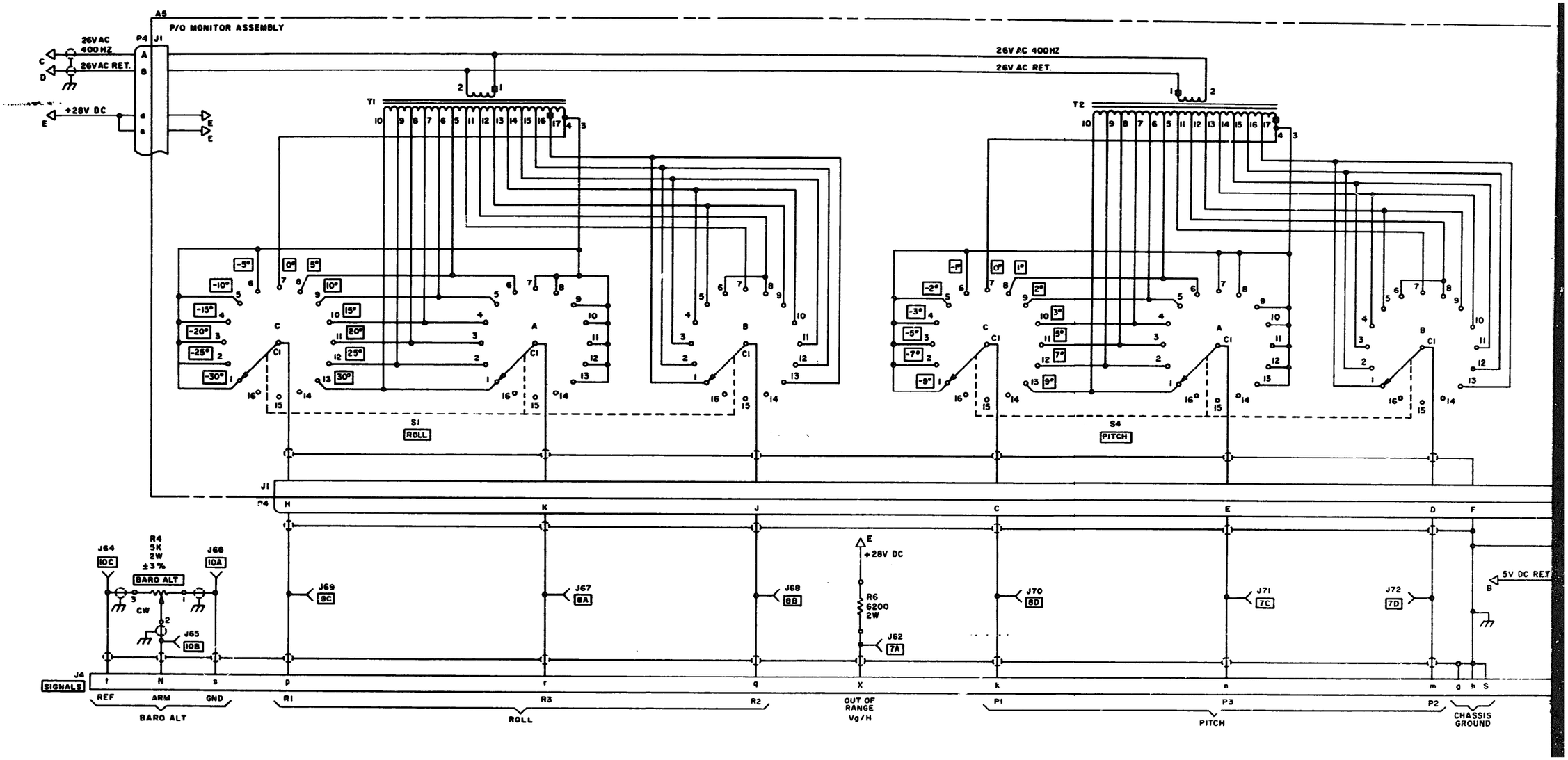


Figure FO-9@. Test set, schematic diagram (part 5 of 5).

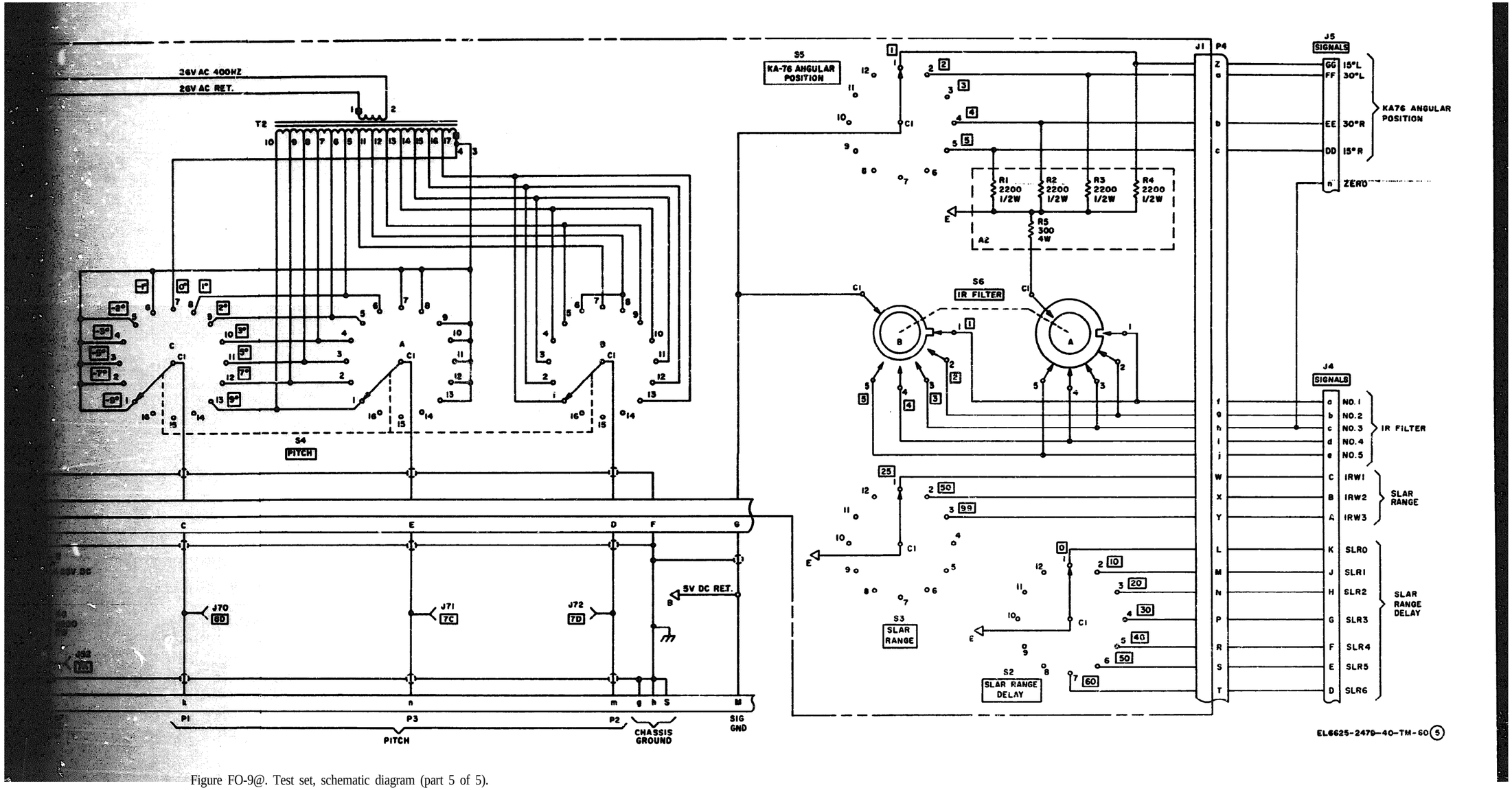
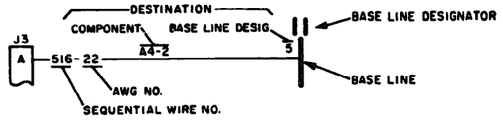


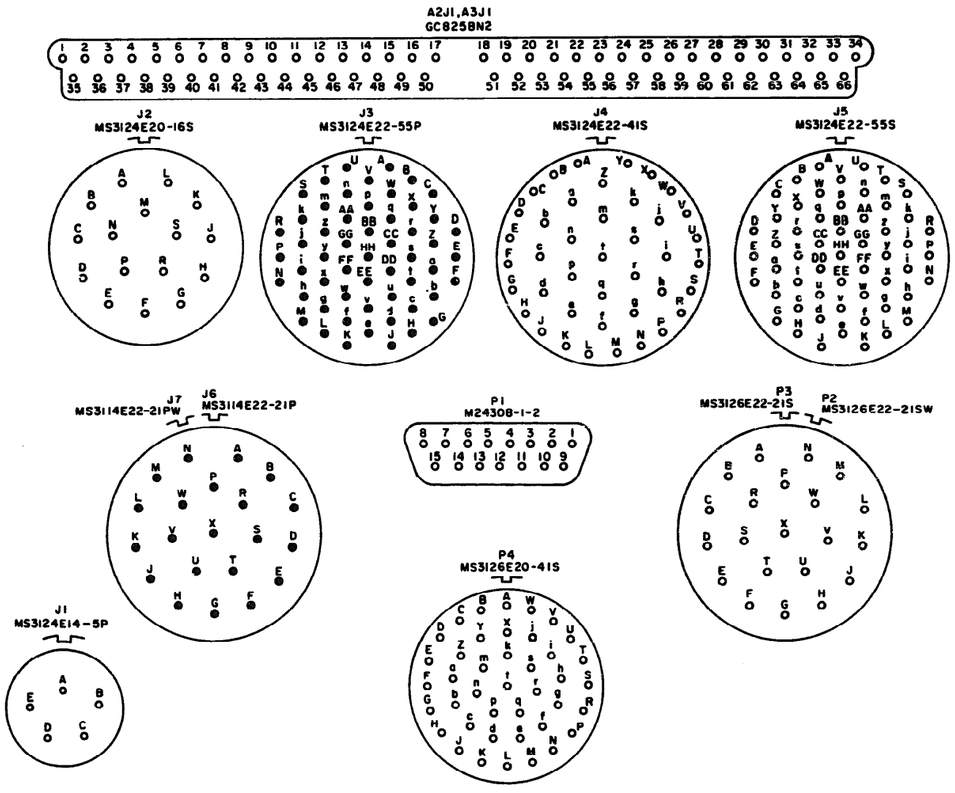
Figure FO-9@. Test set, schematic diagram (part 5 of 5).

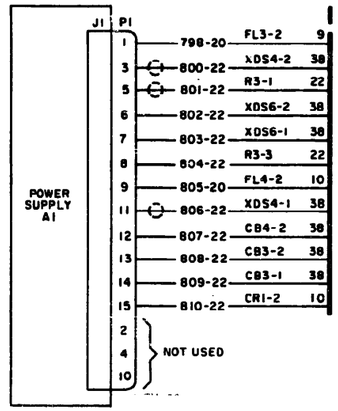
NOTES

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN FOR COMPLETE DESIGNATION, PREFIX WITH IA3.
2. LEGEND FOR BASE-LINE CONNECTION DIAGRAM:



3. POINT-TO-POINT WIRING WITH WIRE LENGTH AS SHORT AS POSSIBLE.
4. CONNECTORS VIEWED FROM FRONT FACE.





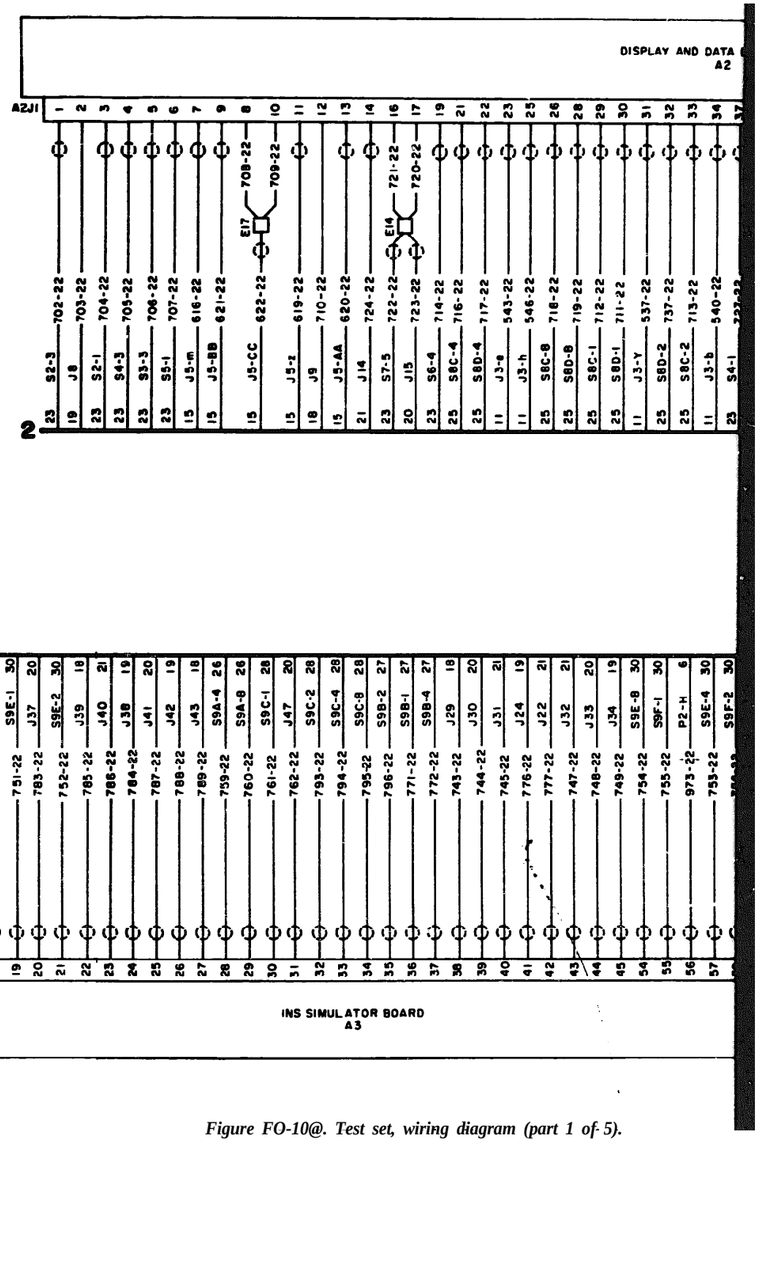


Figure FO-10@. Test set, wiring diagram (part 1 of 5).

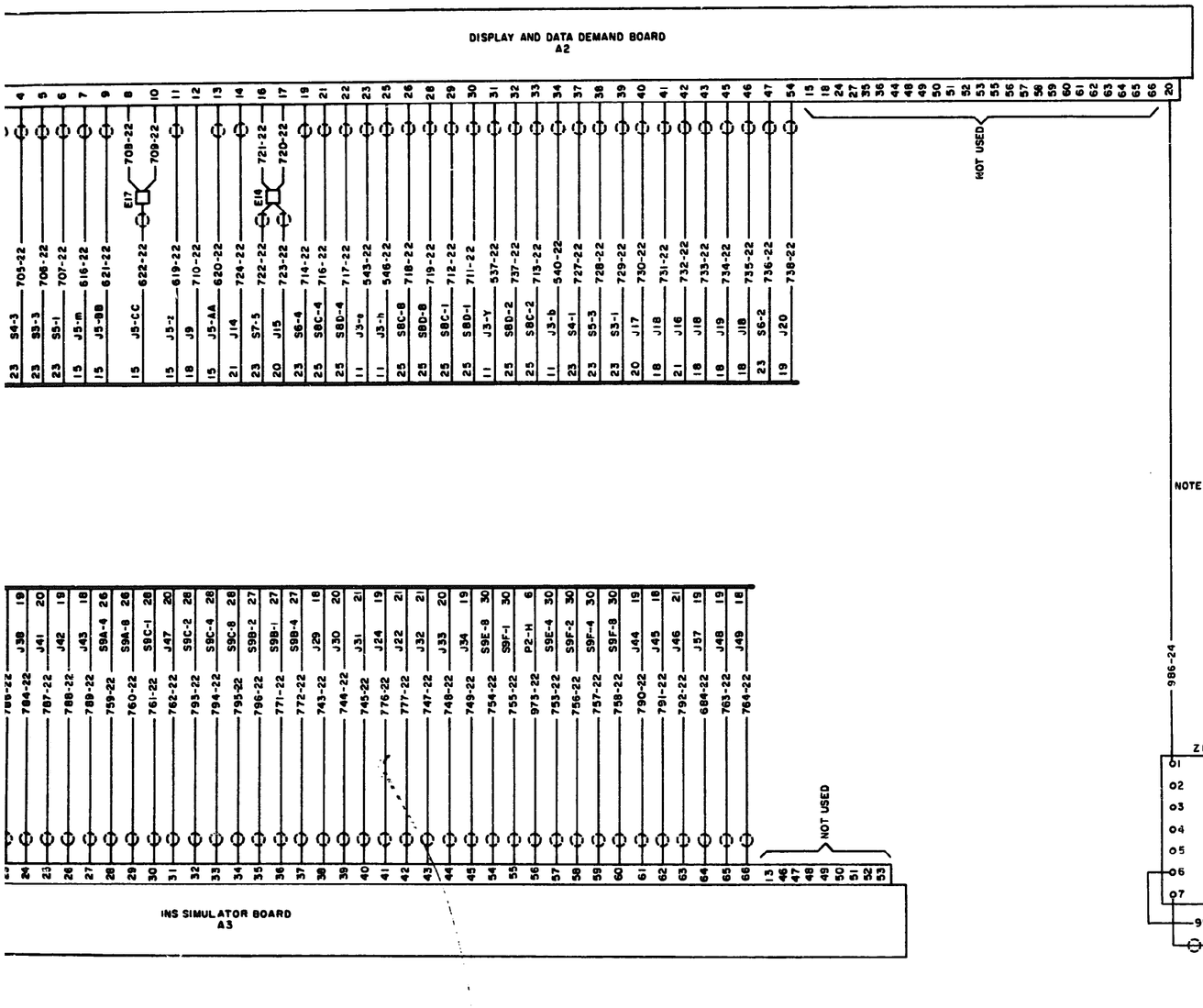
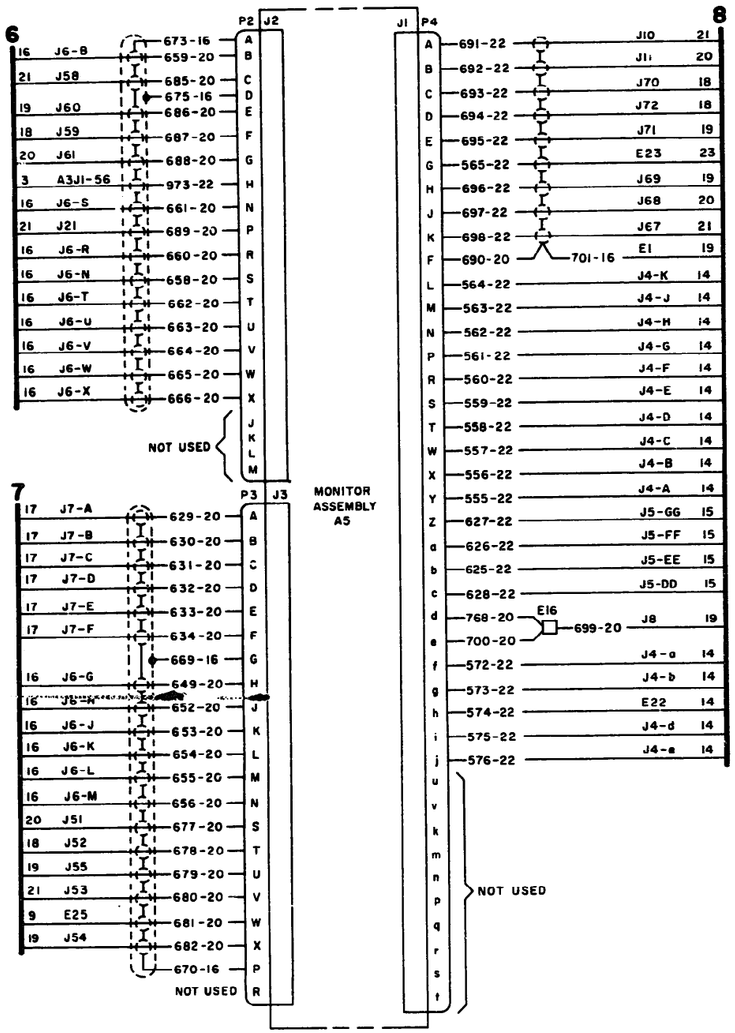


Figure FO-10. Test set, wiring diagram (part 1 of 5).



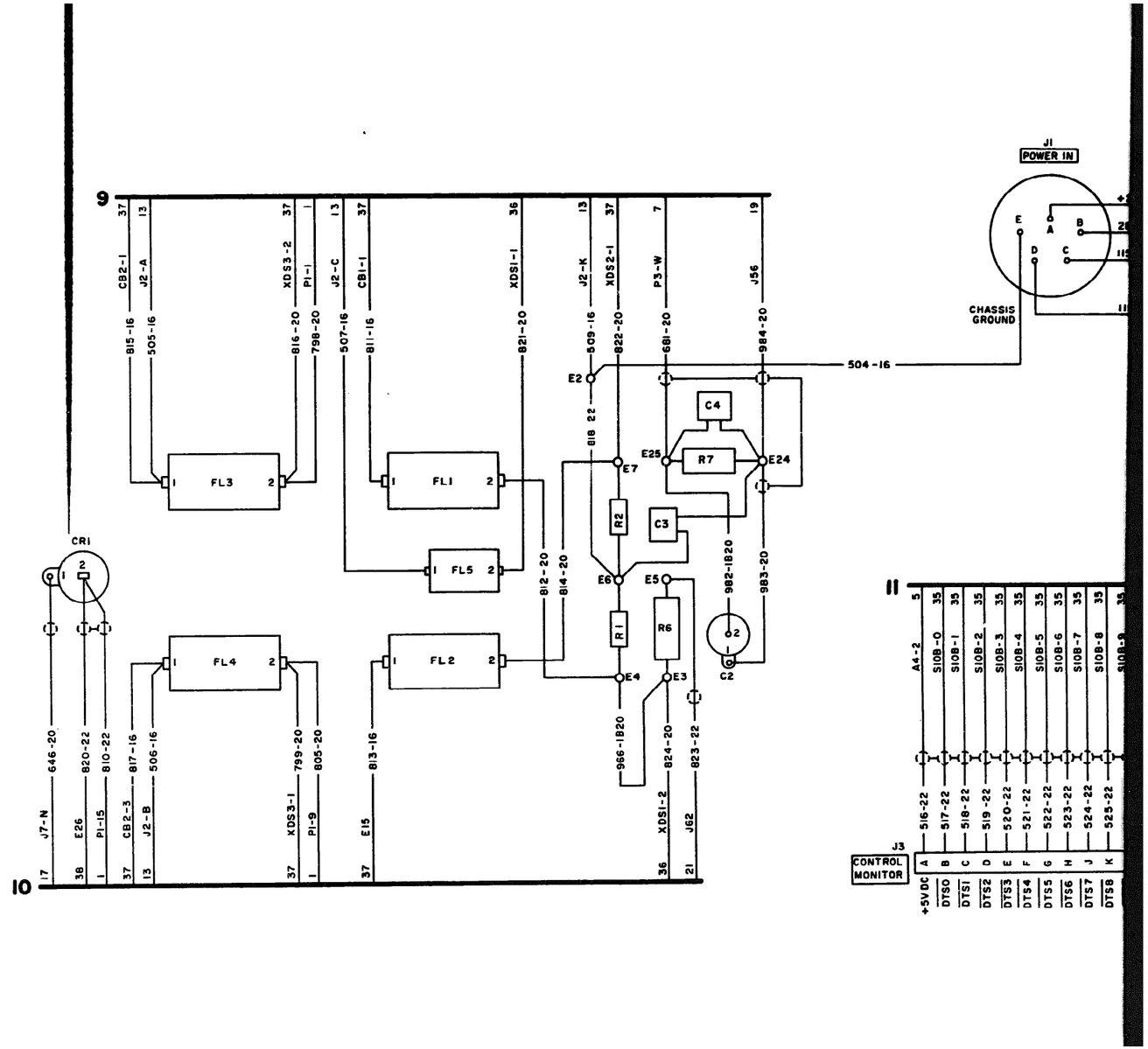


Figure FO-10. Test set, wiring diagram (part 2 of 5).

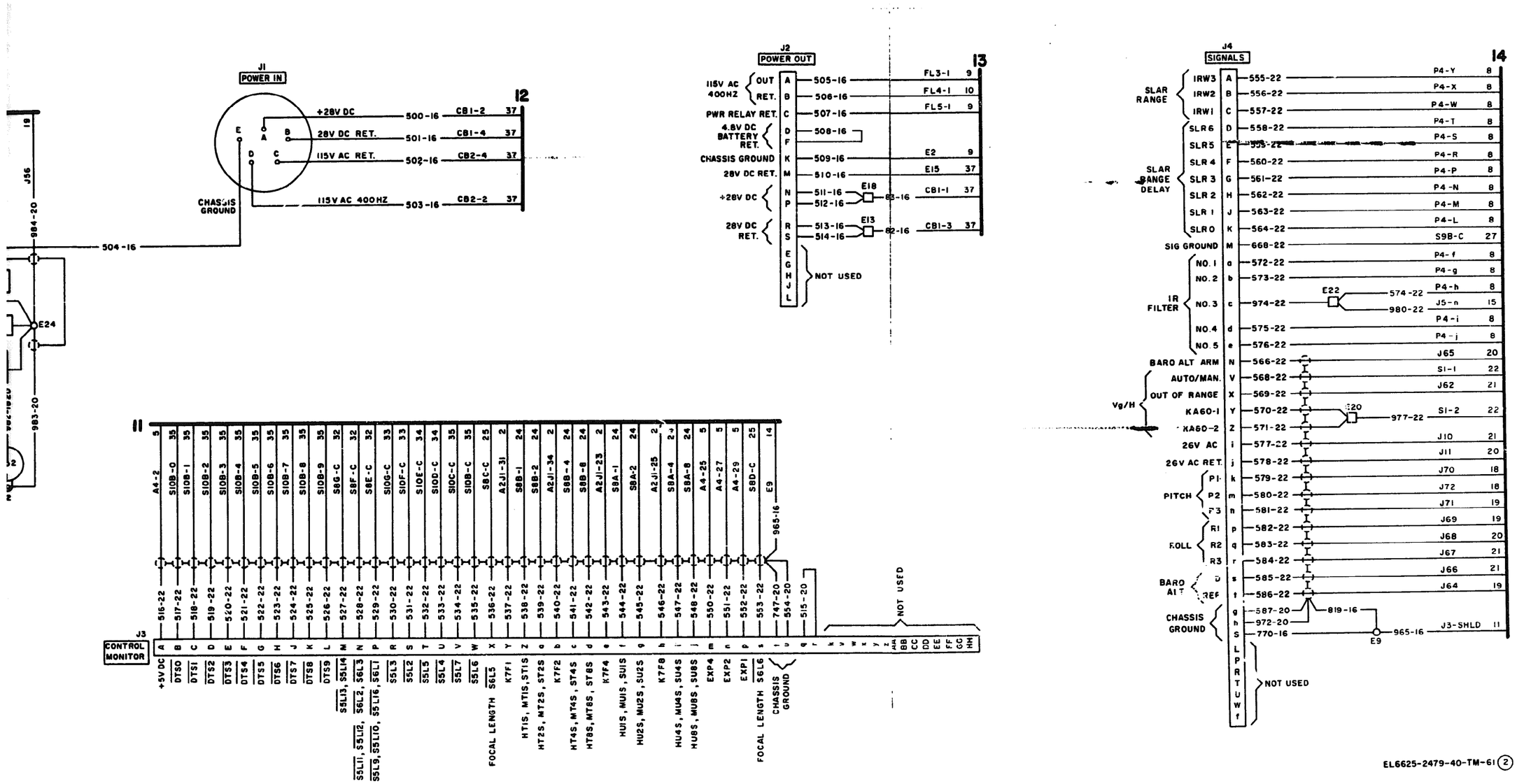


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Figure FO-10@. Test set, wiring diagram (part 2 of 5).

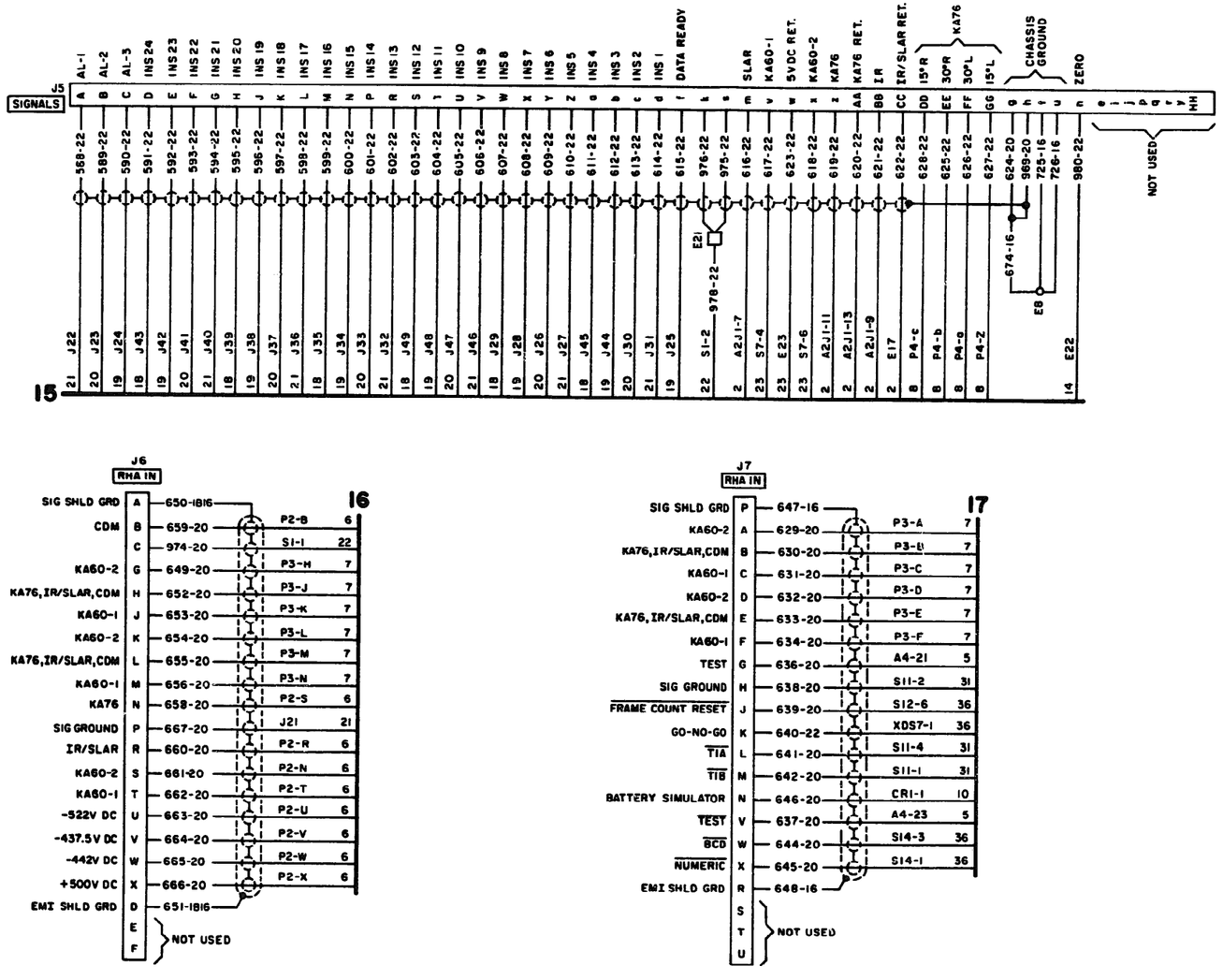


Figure FO-10@. Test ret, wiring diagram (part 8 of 5).

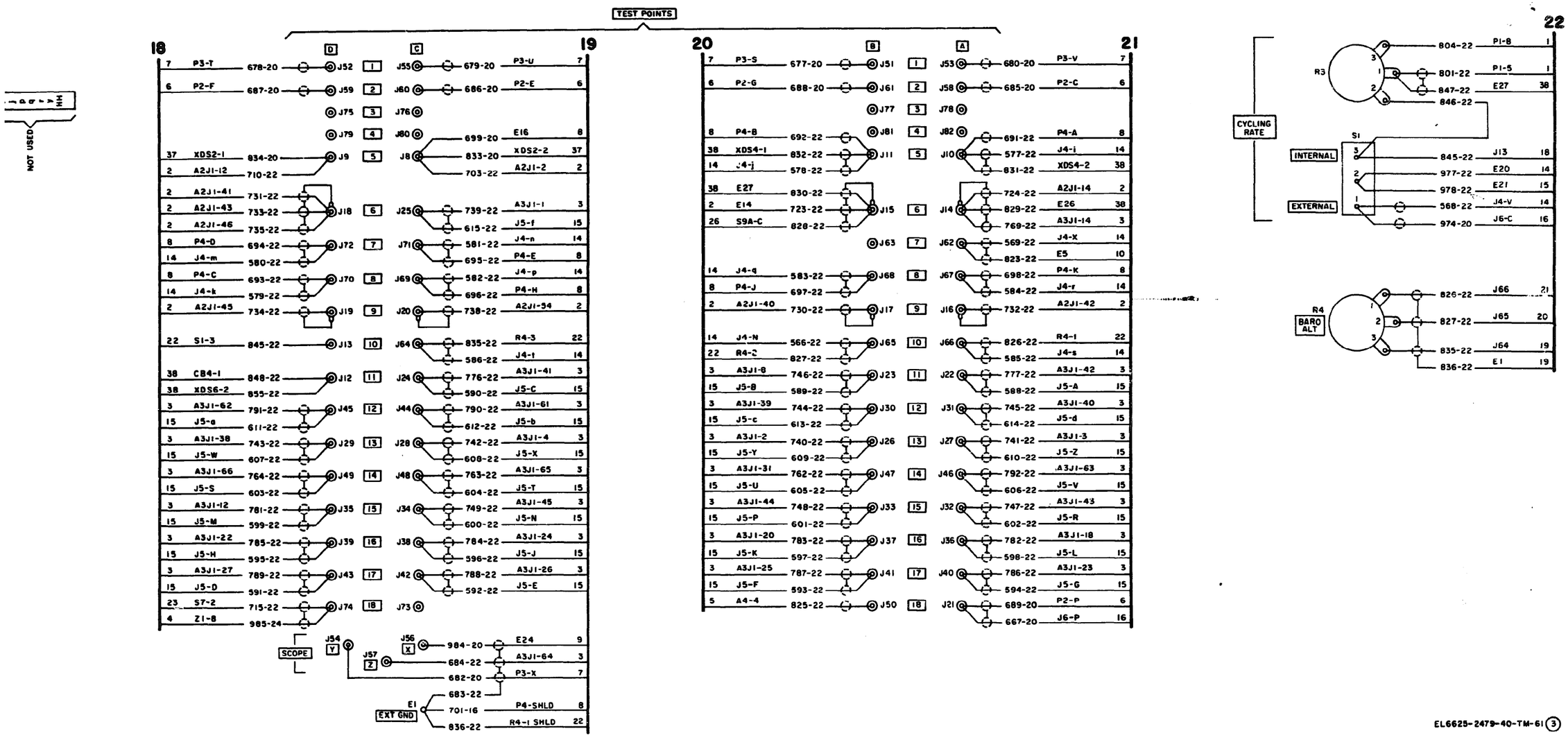


Figure FO-10@. Test set, wiring diagram (part 3 of 5).

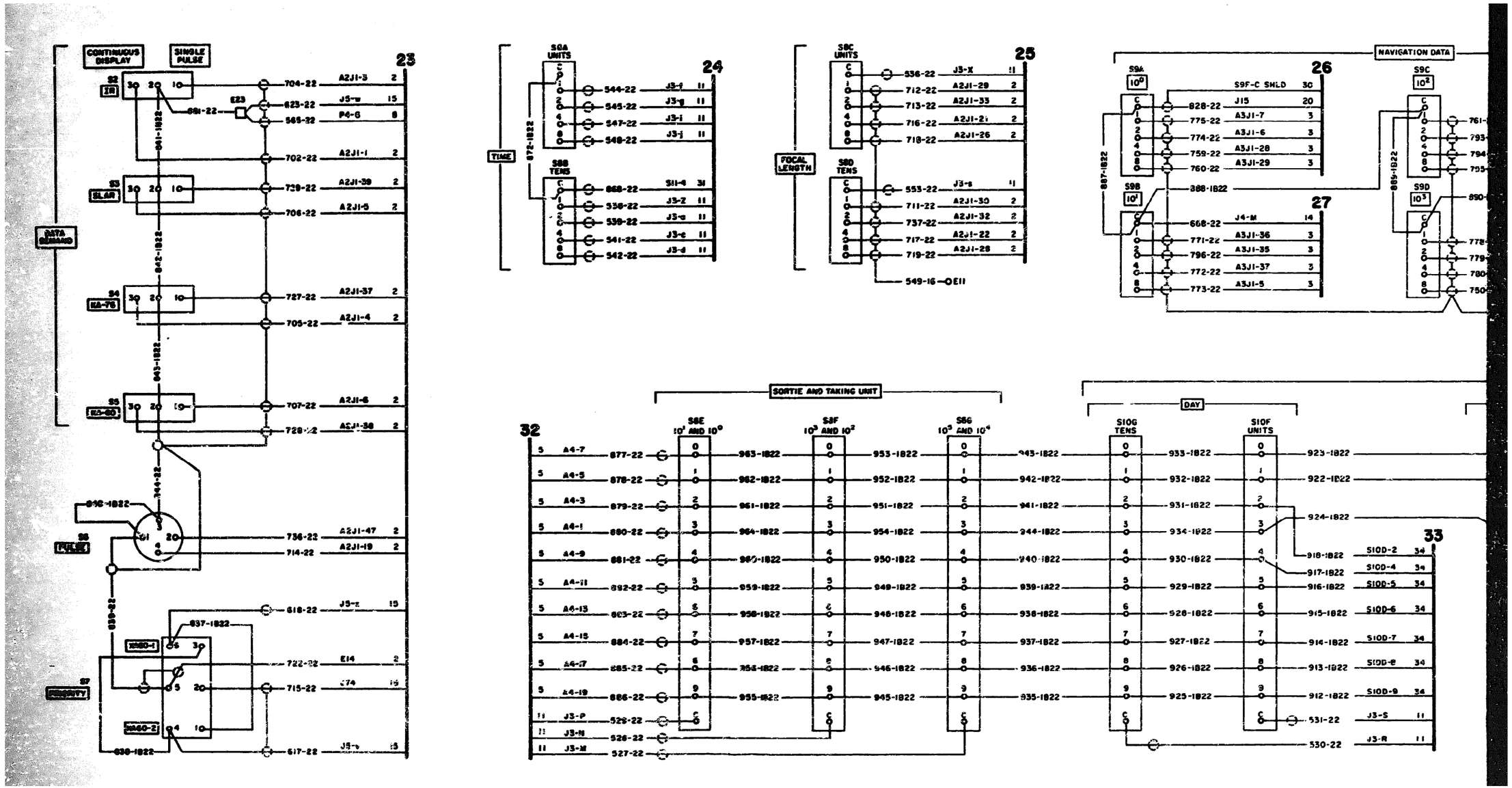


Figure FO-10. Test set, wiring diagram (part 4 of 5).

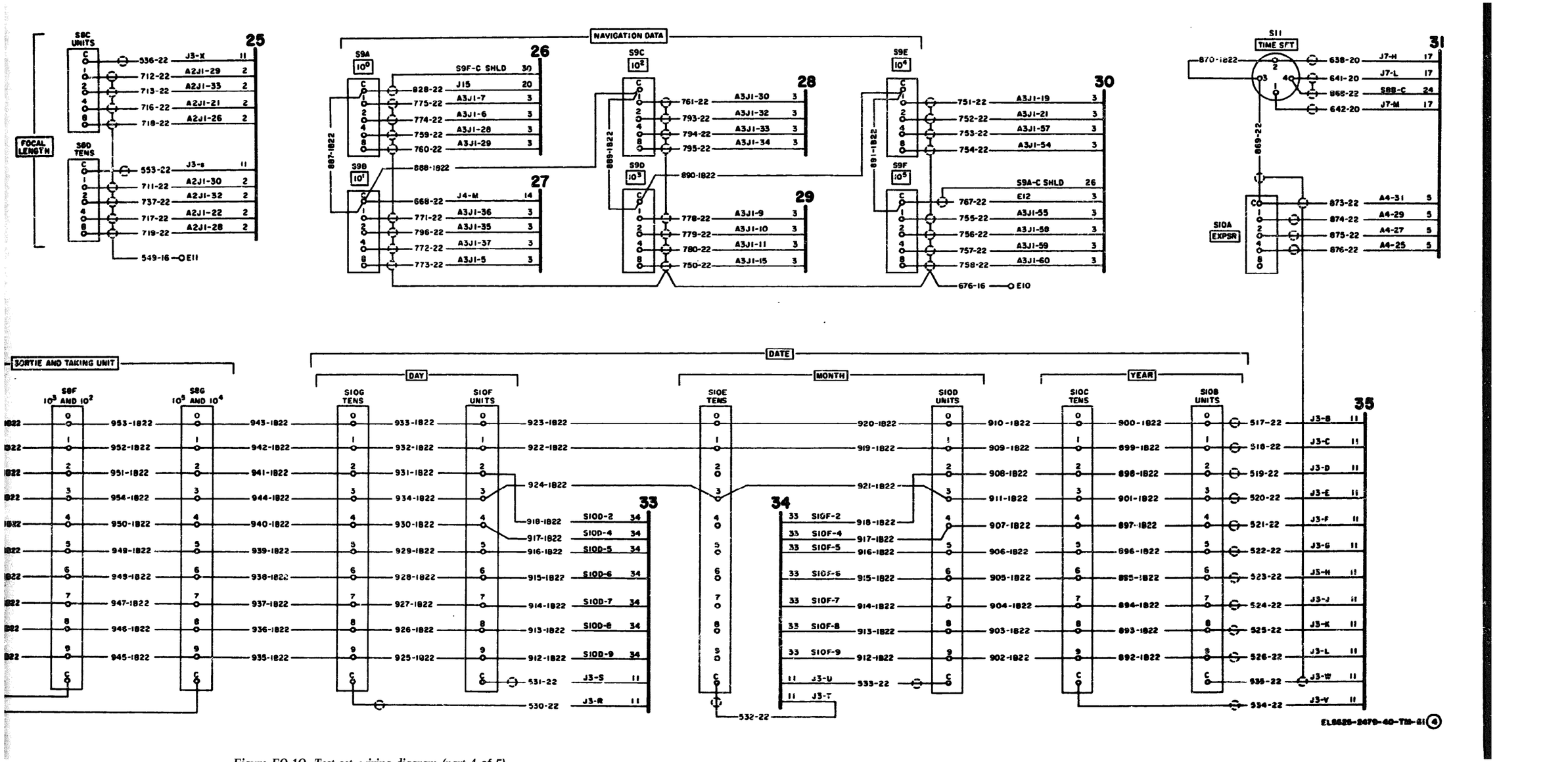


Figure FO-10. Test set, wiring diagram (part 4 of 5).

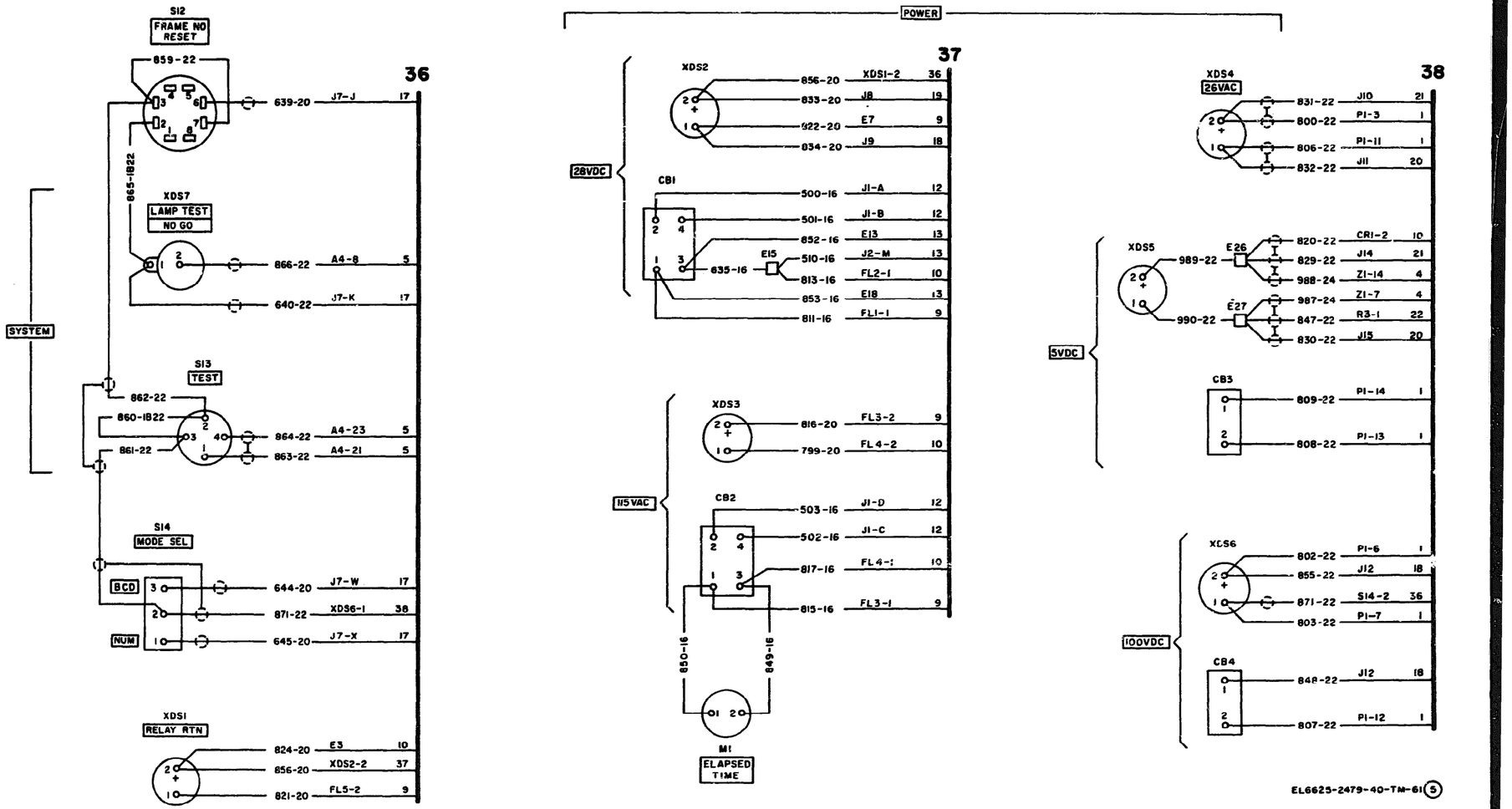


Figure FO-lO@. Test set, wiring diagrams (part 5 of 5).

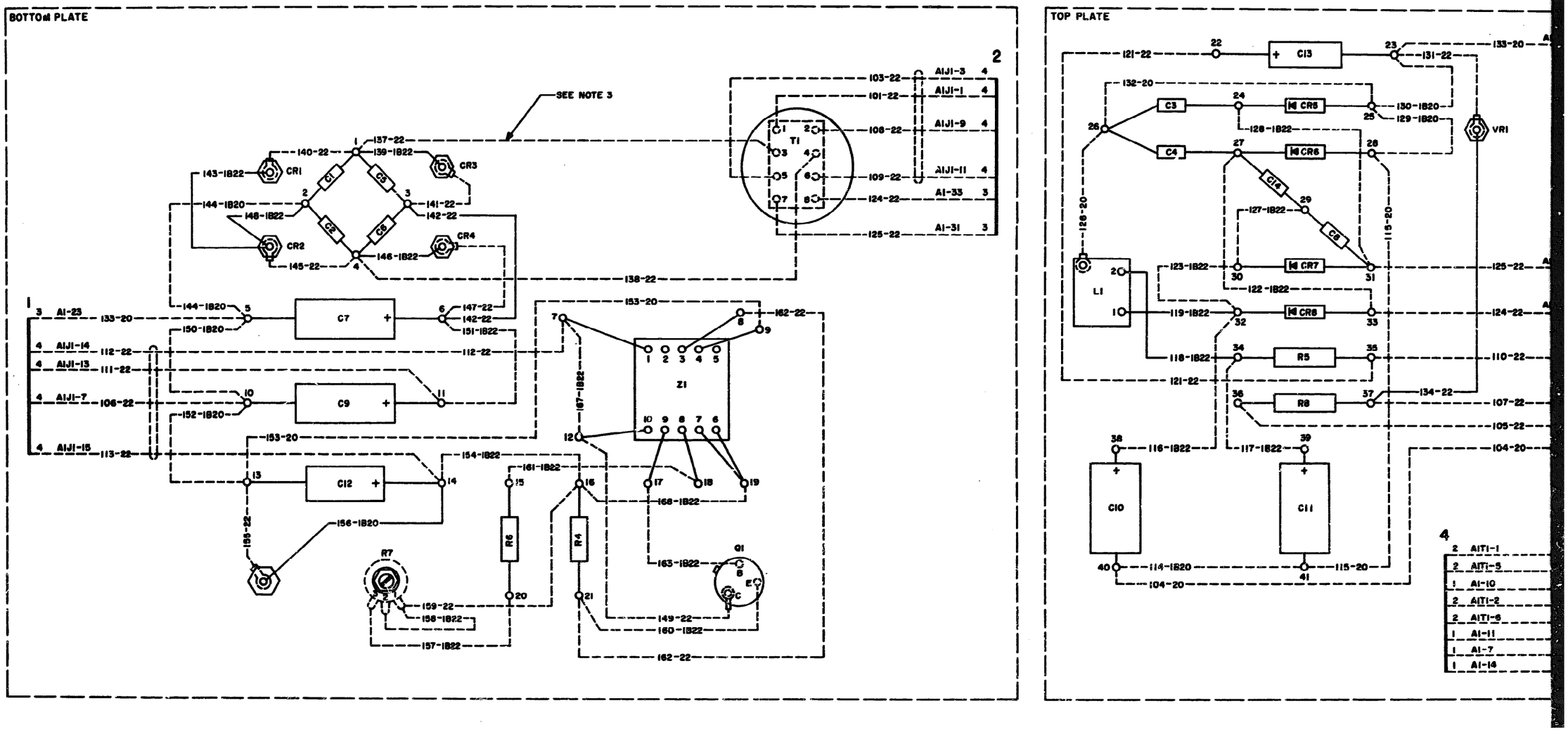
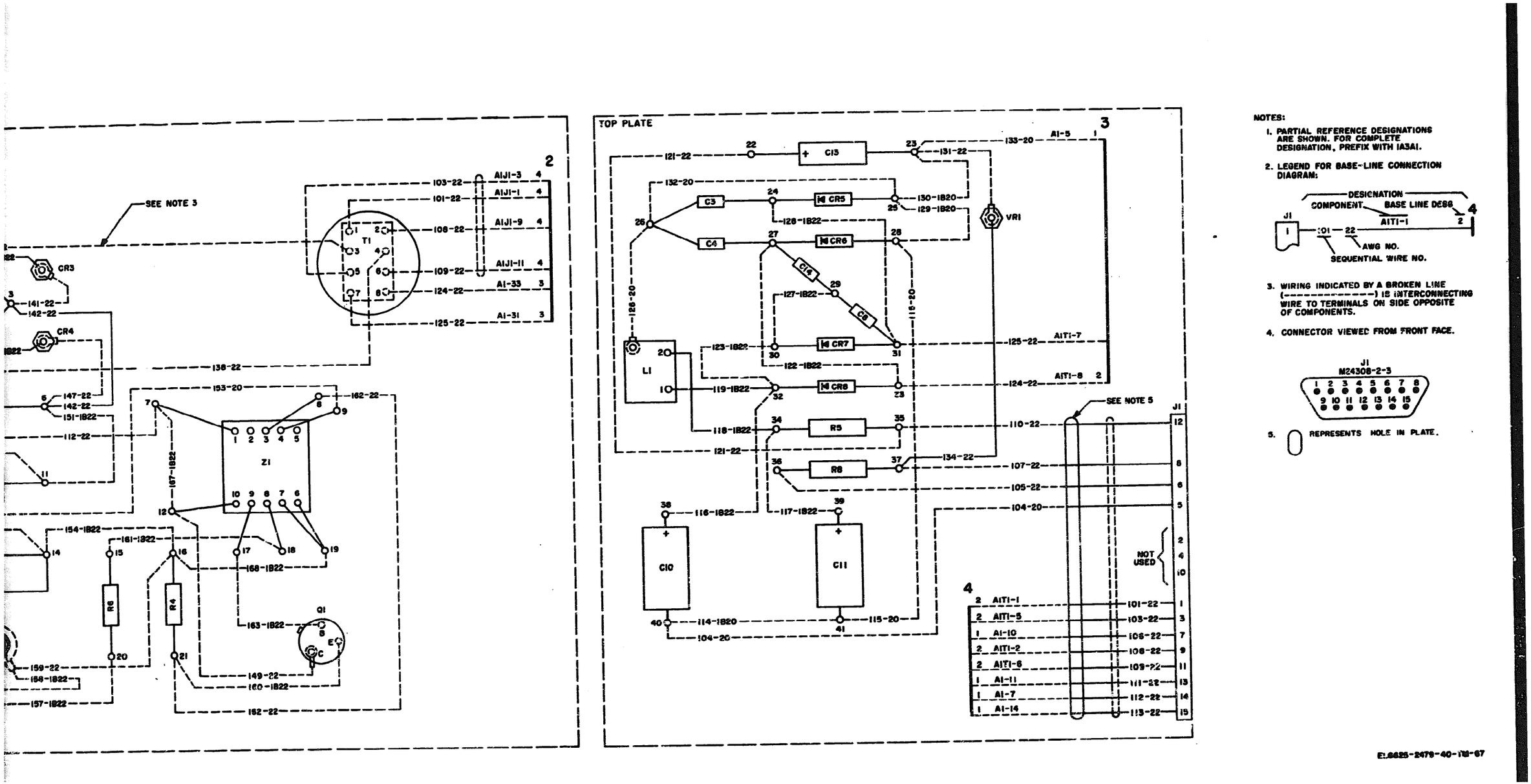


Figure FO-11. Power supply, wiring diagrams.



NOTES:

1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN. FOR COMPLETE DESIGNATION, PREFIX WITH 1A5A1.
2. LEGEND FOR BASE-LINE CONNECTION DIAGRAM:

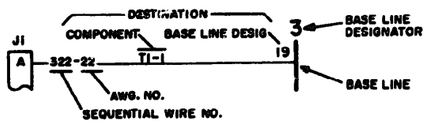
3. WIRING INDICATED BY A BROKEN LINE (- - - - - - - - - - - - - -) IS INTERCONNECTING WIRE TO TERMINALS ON SIDE OPPOSITE OF COMPONENTS.
4. CONNECTOR VIEWED FROM FRONT FACE.

5. 0 REPRESENTS HOLE IN PLATE.

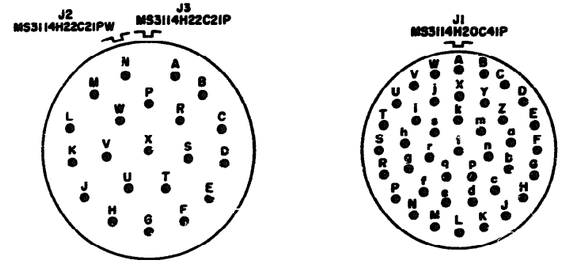
Figure FO-11. Power supply, wiring diagram.

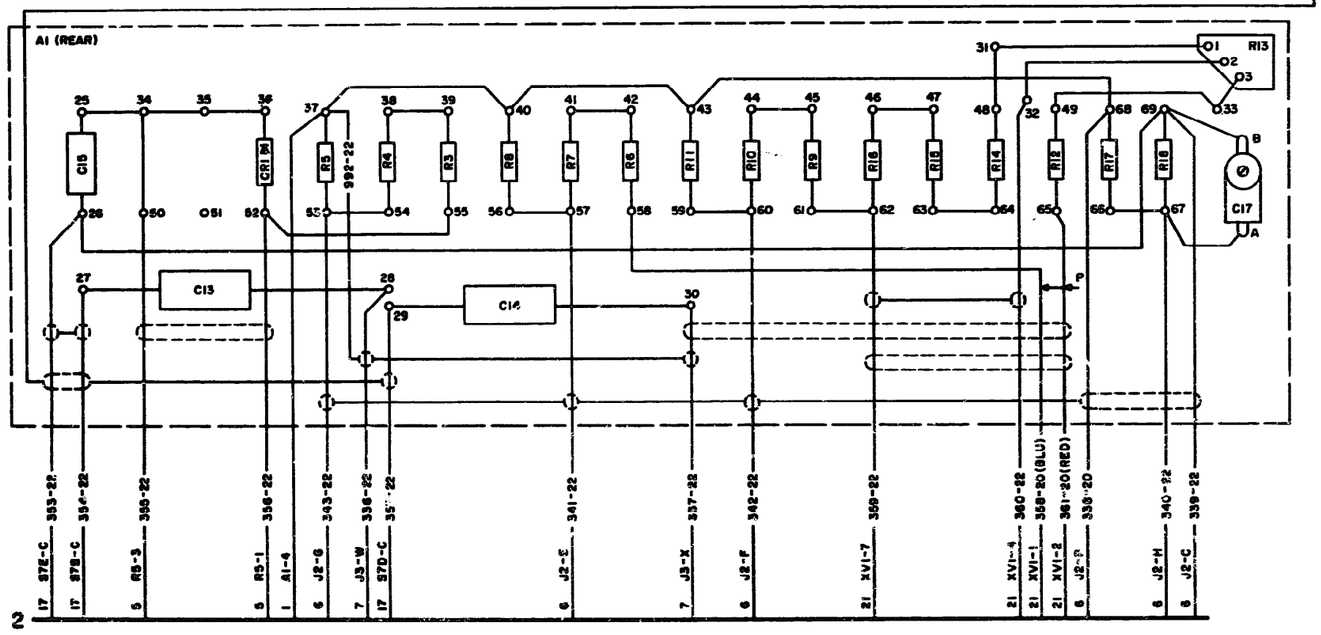
NOTES:

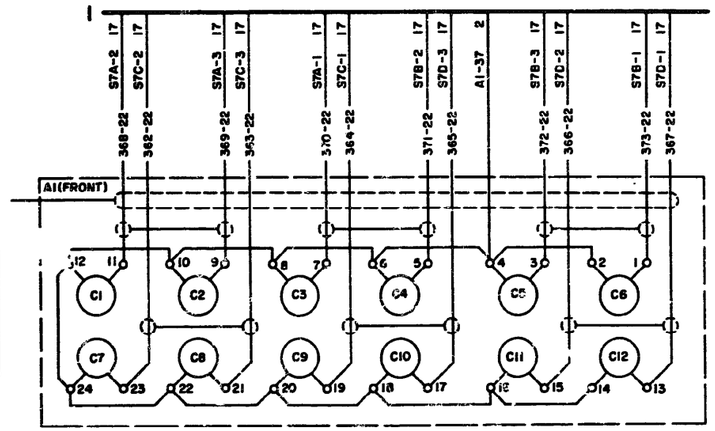
1. PARTIAL REFERENCE DESIGNATIONS ARE SHOWN FOR COMPLETE DESIGNATION, PREFIX WITH 1A3A5.
2. LEGEND FOR BASE-LINE CONNECTION DIAGRAM:

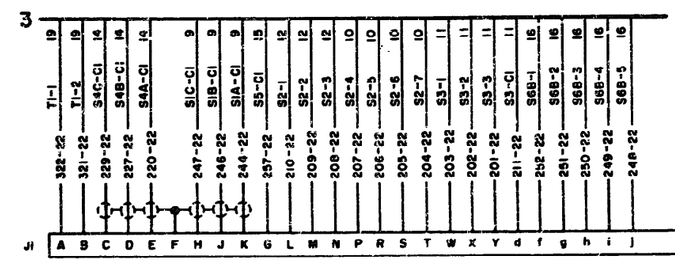


3. POINT-TO-POINT WIRING WITH WIRE LENGTH AS SHORT AS POSSIBLE.
4. CONNECTORS VIEWED FROM FRONT FACE:









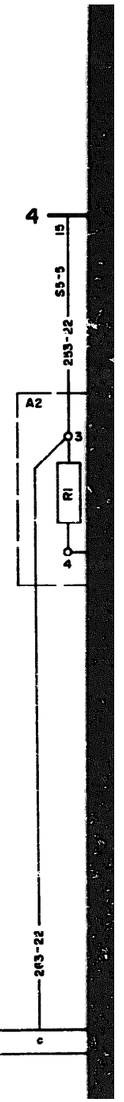
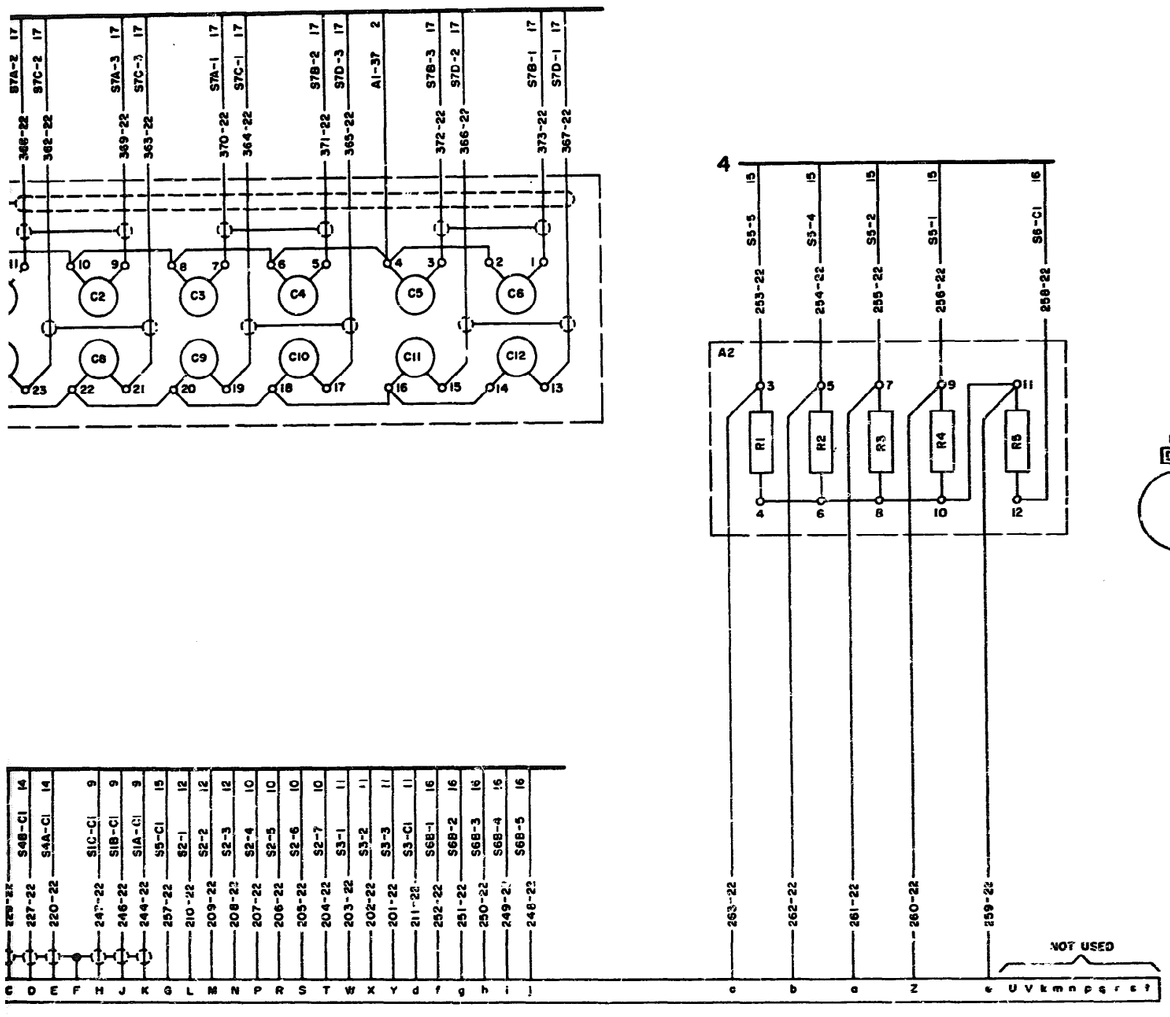
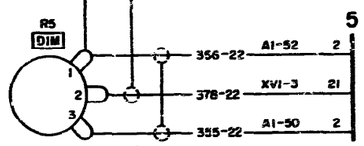


Figure FO-12. Monitor assembly, wiring diagram (part 1 of 3).





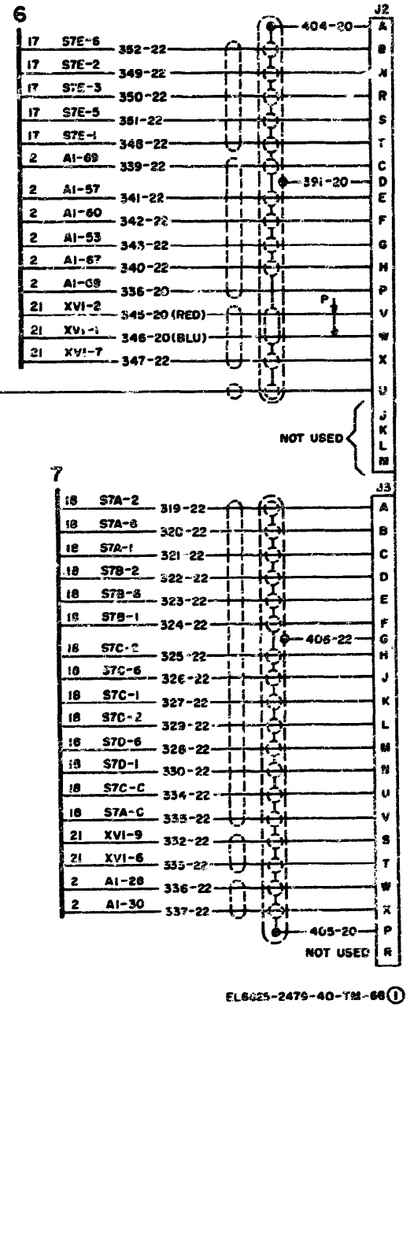


Figure FO-12@. Monitor assembly, wiring diagram (part 1 of 3).

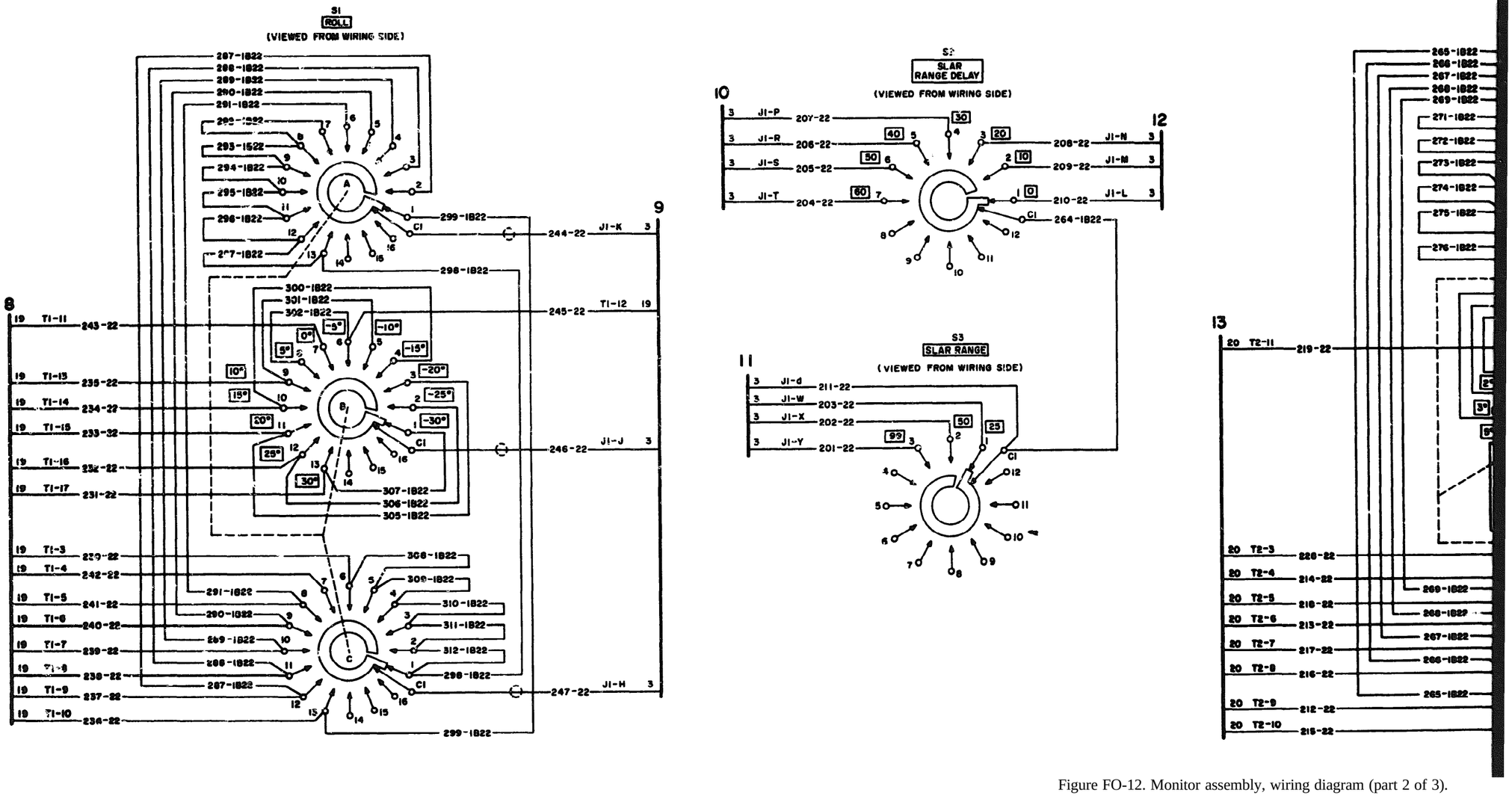


Figure FO-12. Monitor assembly, wiring diagram (part 2 of 3).

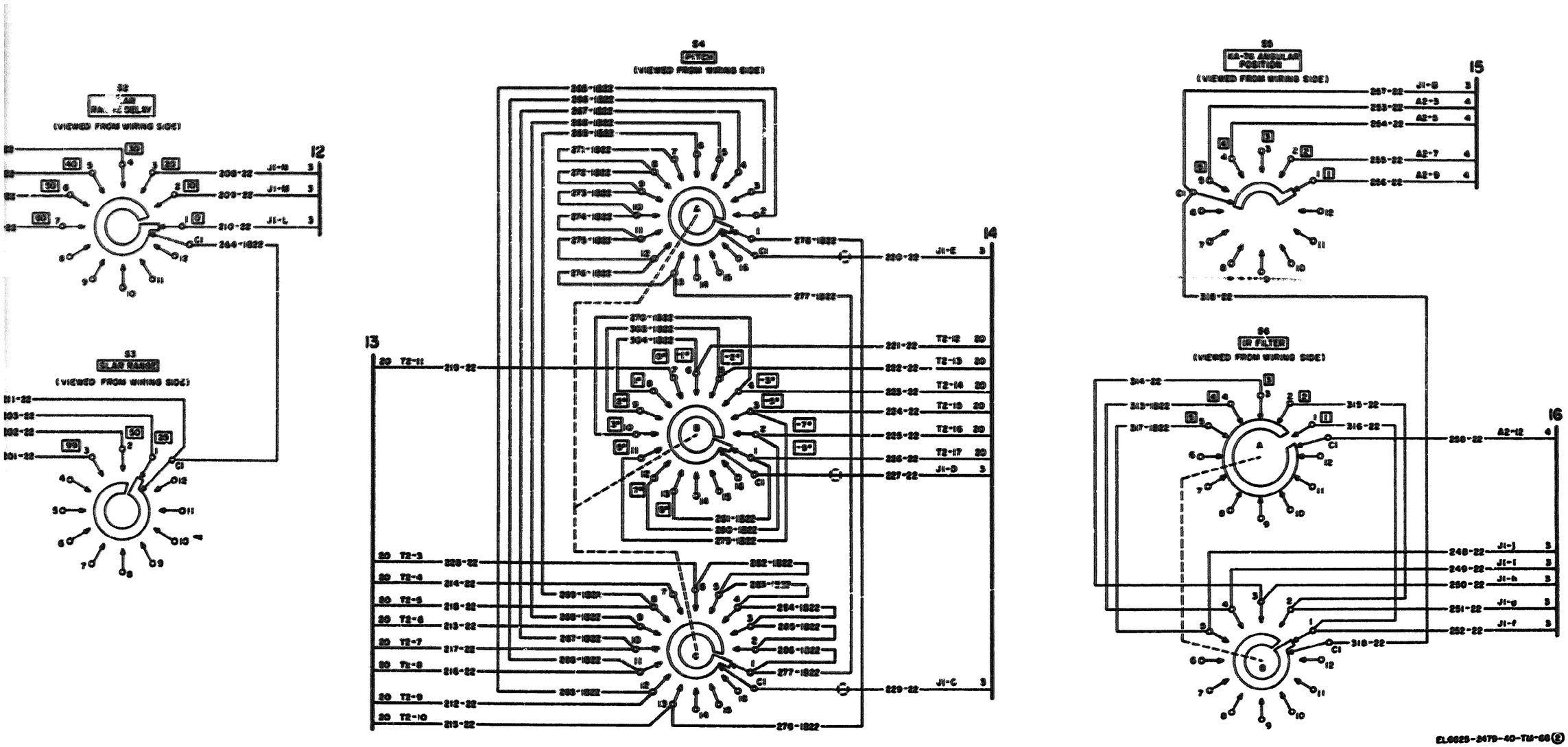


Figure FO-10. Monitor assembly, wiring diagram (part 2 of 3).

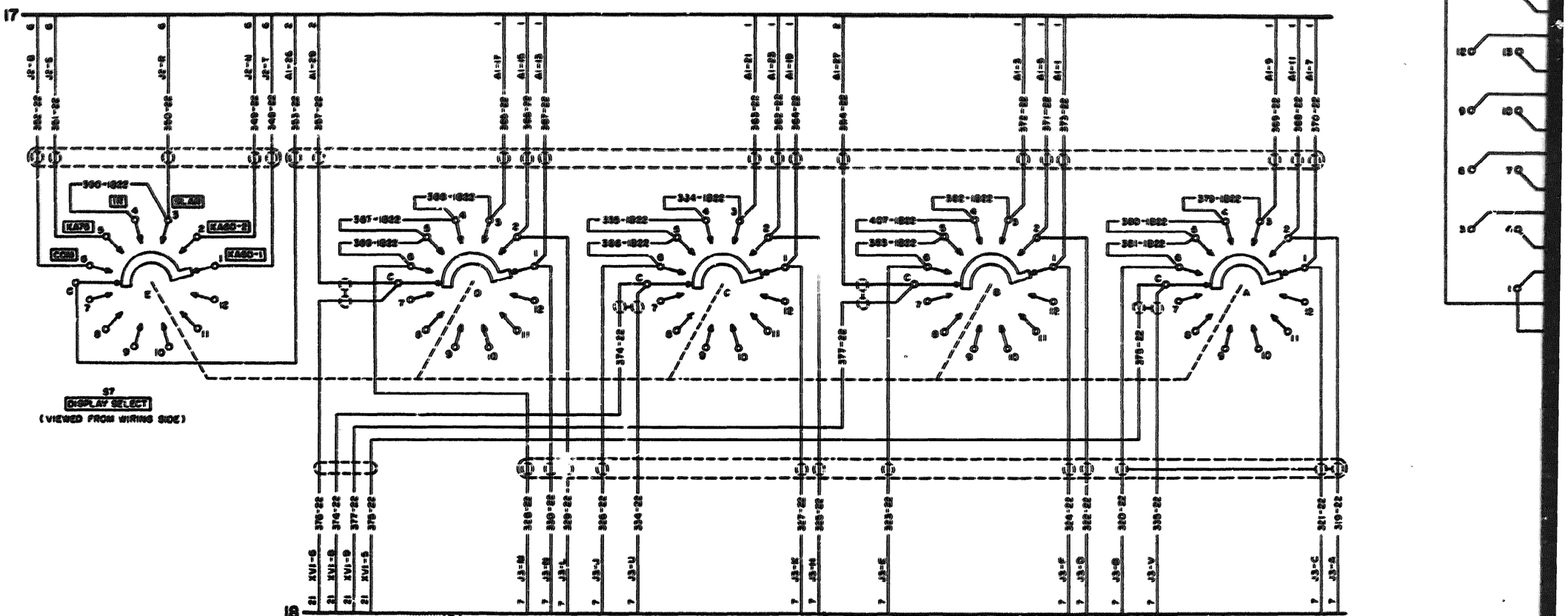
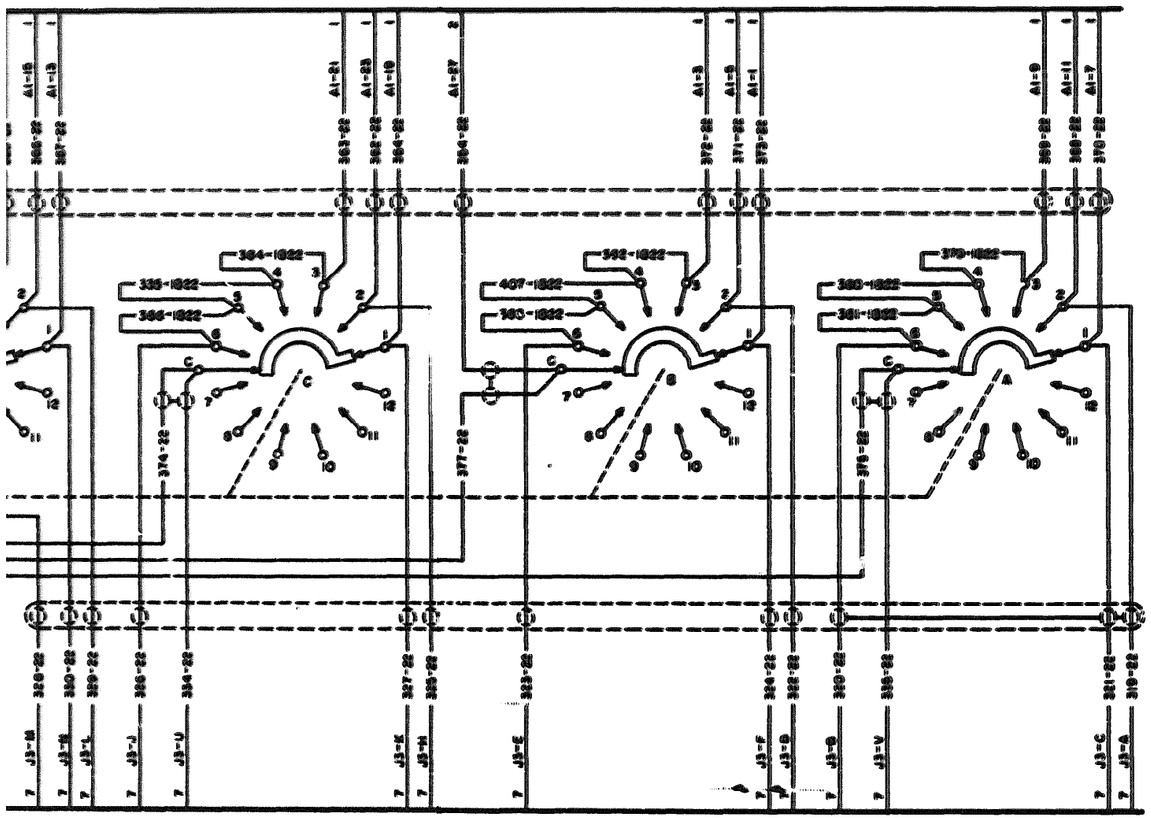


Figure FO-12. Monitor assembly, wiring diagram (part 3 of 3).



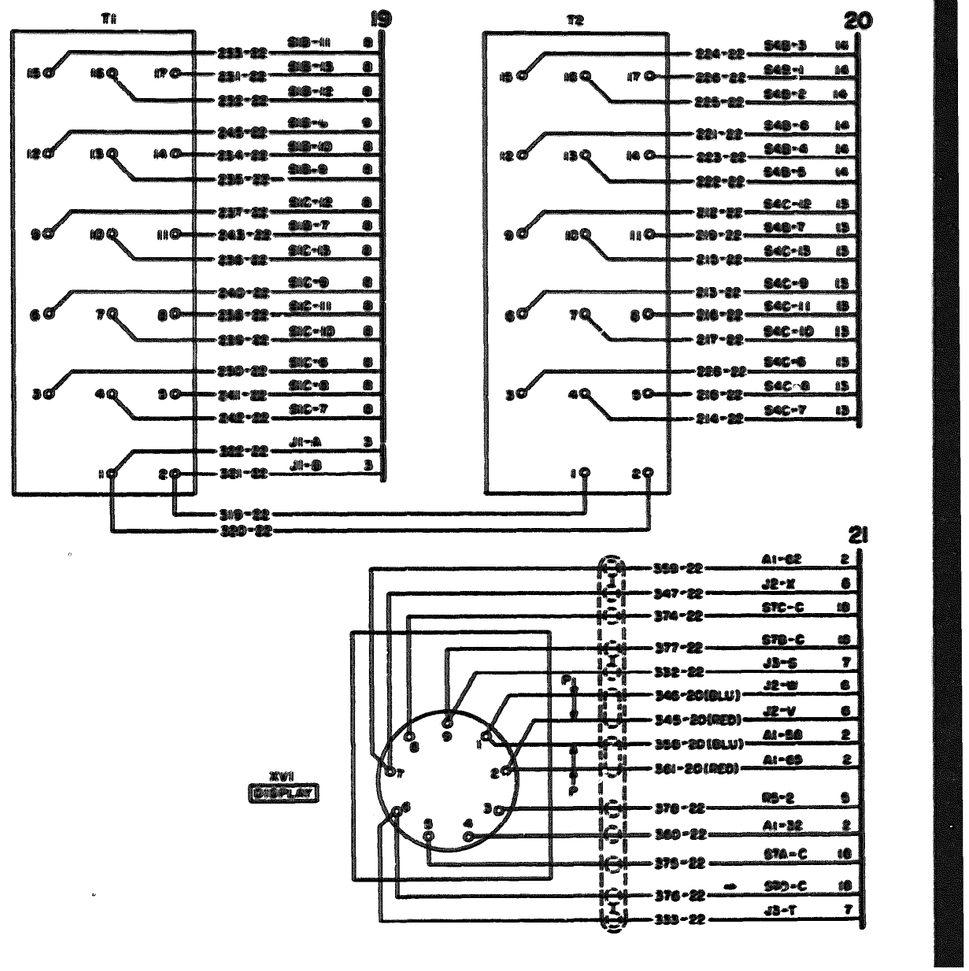


Figure FO-12. Monitor assembly, wiring diagram (part 3 of 3).

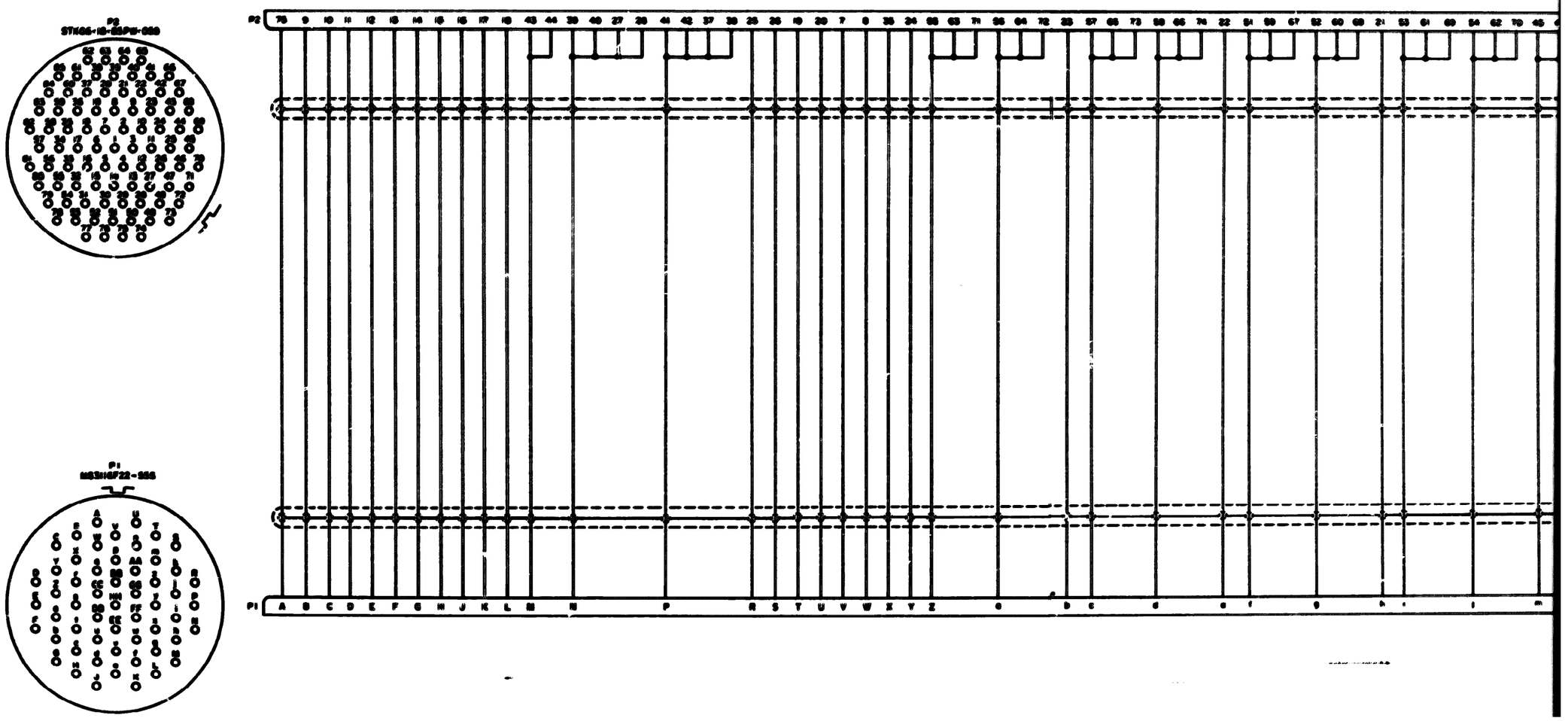
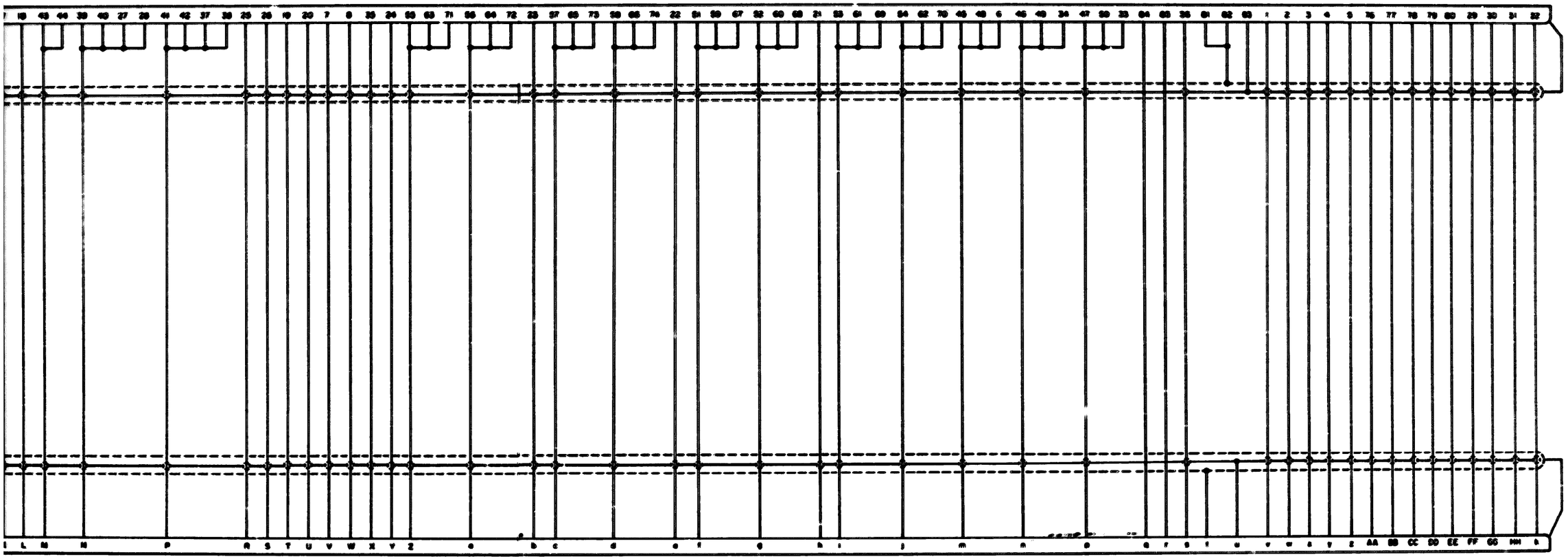


Figure FO-13. Cable Assembly, Special Purpose, Electrical CX-12715/AYM-3. wiring diagram.



NOTES:
1. REFERENCE DESIGNATIONS ARE ABBREVIATED. PREFIX THE REFERENCE DESIGNATION WITH 2W2.
2. ALL WIRES ARE NO. 22 AWG.

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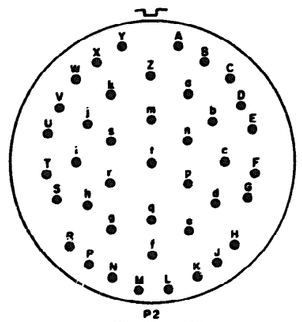
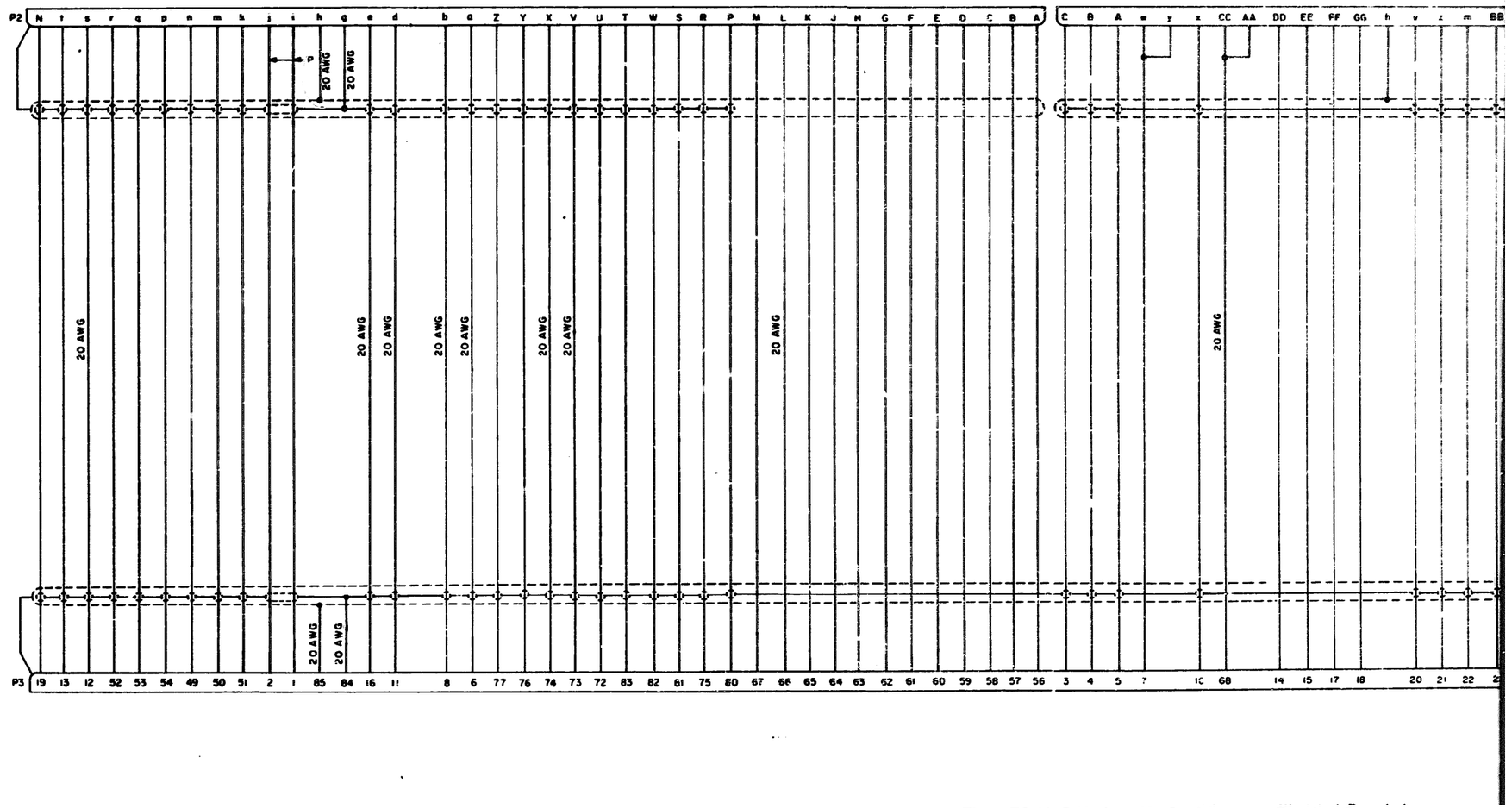
Figure FO-18. Cable Assembly, Special Purpose, Electrical CX-12716/AYM-6, wiring diagram.





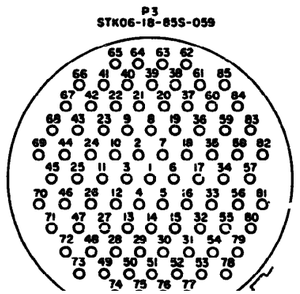
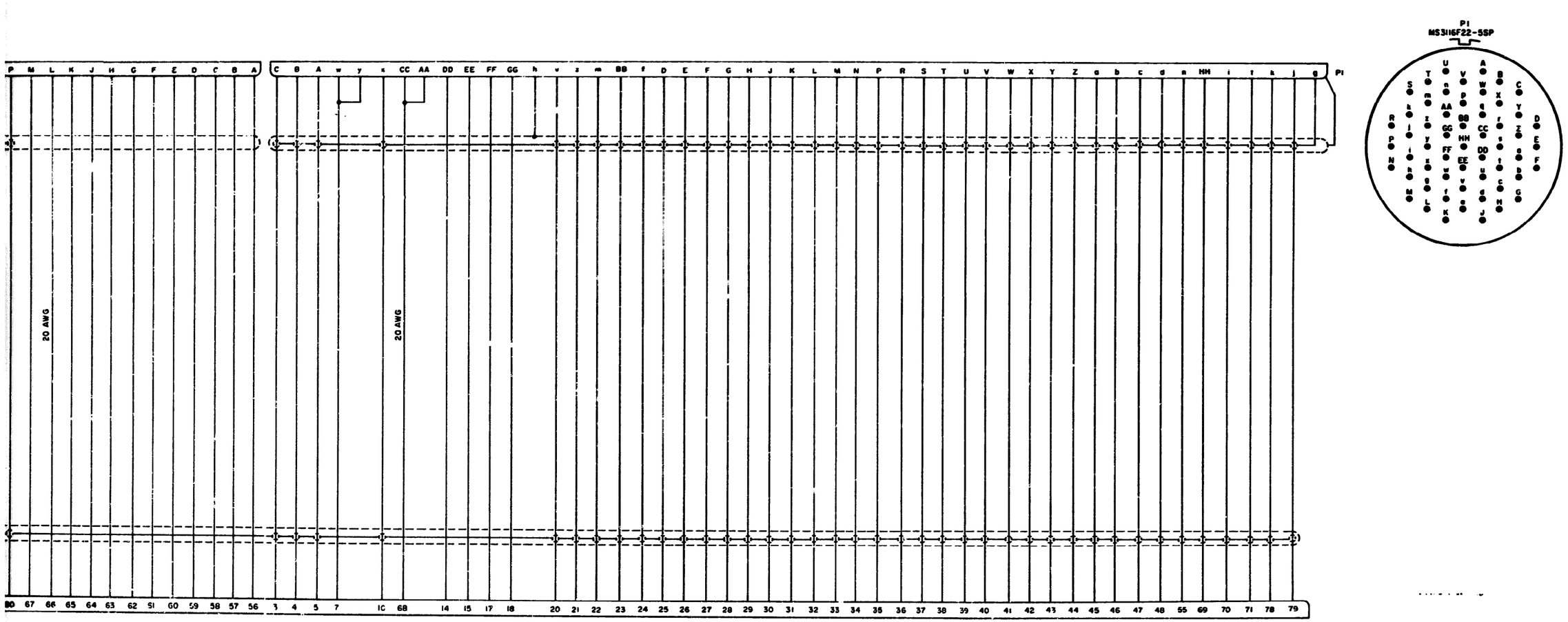


Figure FO-14. Cable Assembly, Special purpose, Electrical, Branched CX-12716/AYM-8, wiring diagram.



NOTES:
1. REFERENCE DESIGNATIONS ARE ABBREVIATED PREFIX THE REFERENCE DESIGNATION WITH 2W3.
2. UNLESS OTHERWISE SPECIFIED ALL WIRES ARE NO. 22 AWG.

Figure FO-14. Cable Assembly, Special purpose, Electrical. Branched
CX-12716/AYB-3, wiring diagram.

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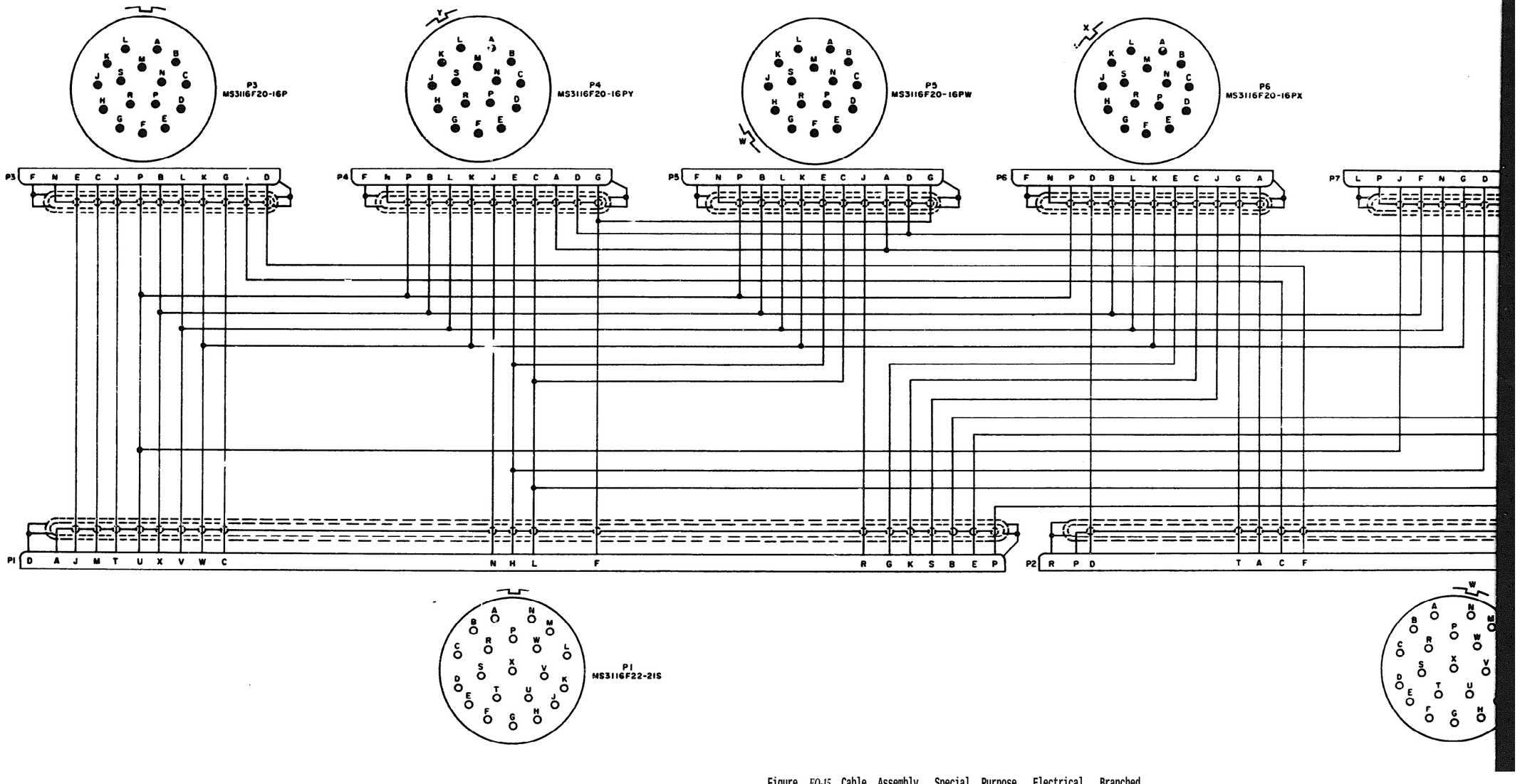


Figure *FO-15.* Cable Assembly, Special Purpose, Electrical, Branched *CX-12717/AYM-8,* wirinq diagram.

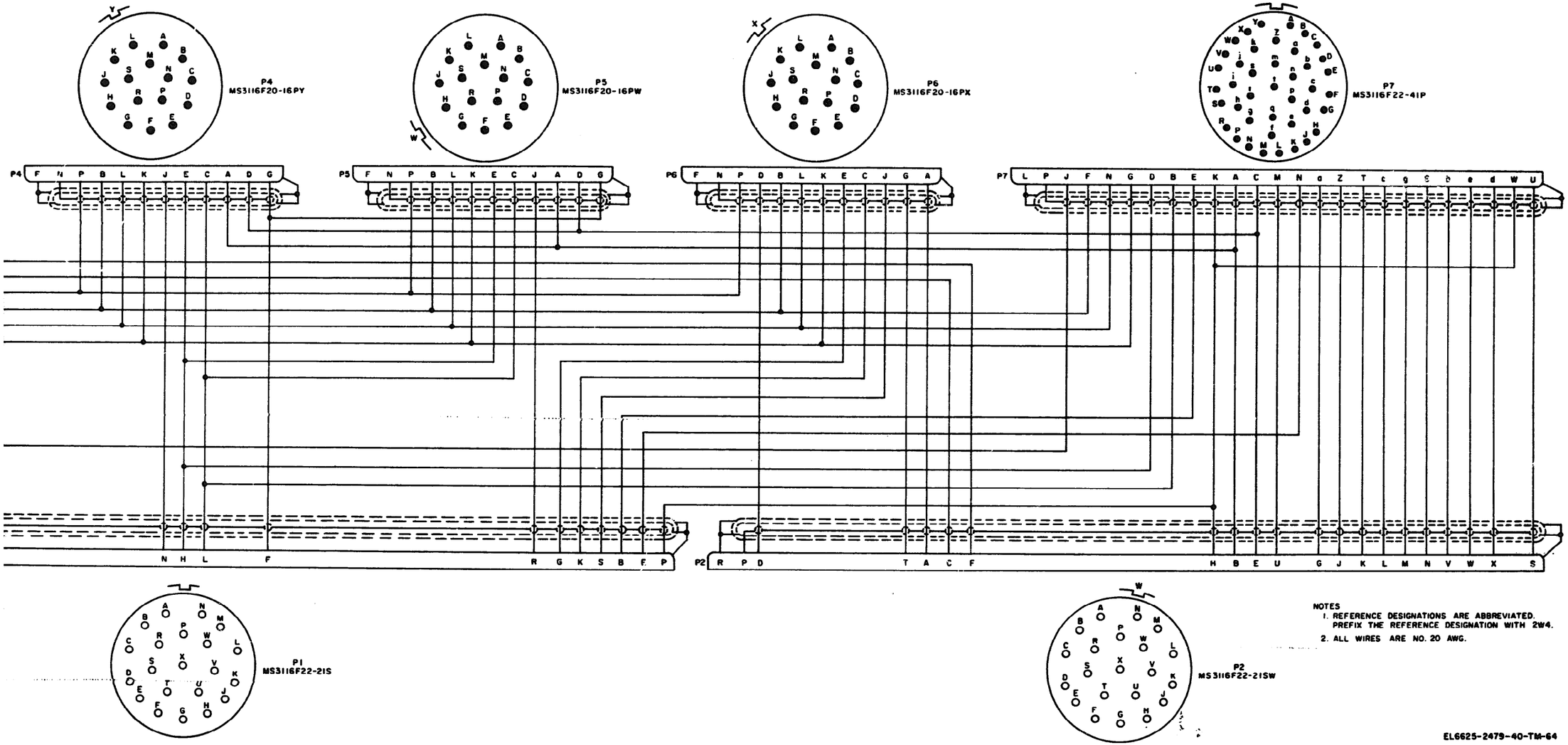


Figure FO-15. Cable Assembly, Special Purpose, Electrical, Branched *CX-12717/AYX-8, wiring diagram.*

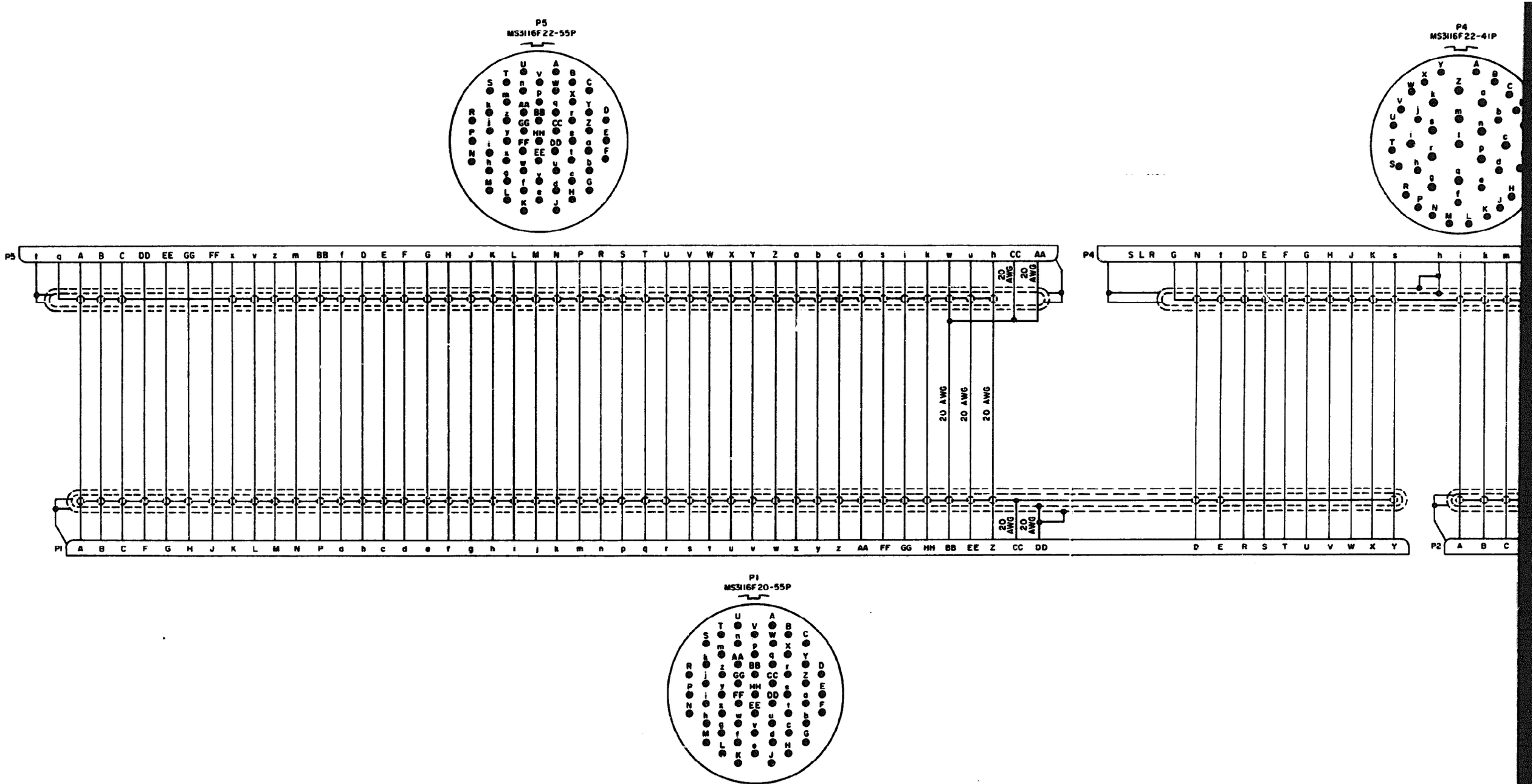


Figure FO-15. Cable Assembly, Special Purpose, Electrical, Branched
Cx-12719/AYM-3 wirimg diagram.

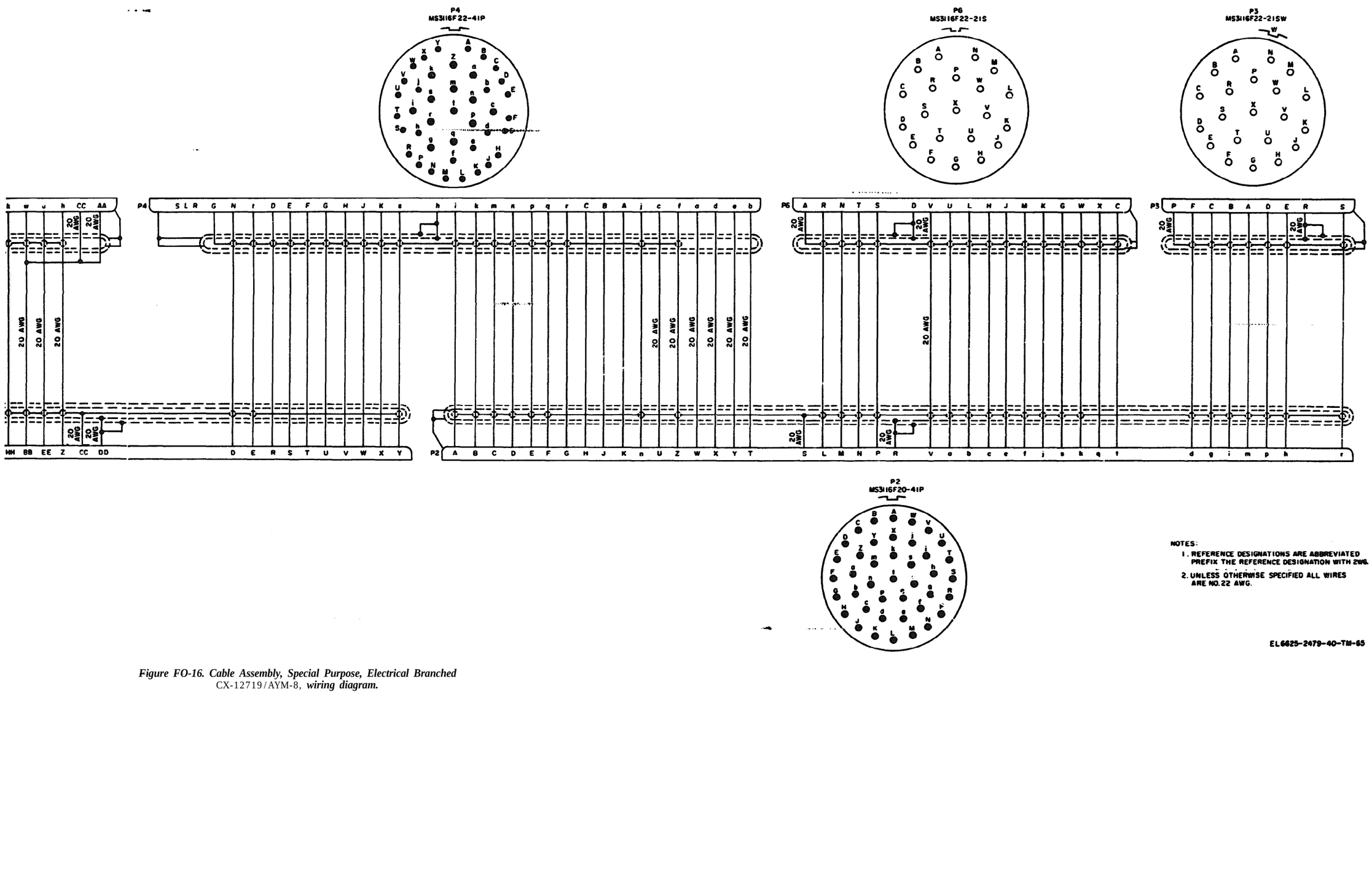


Figure FO-16. Cable Assembly, Special Purpose, Electrical Branched CX-12719/AYM-8, *wiring diagram.*

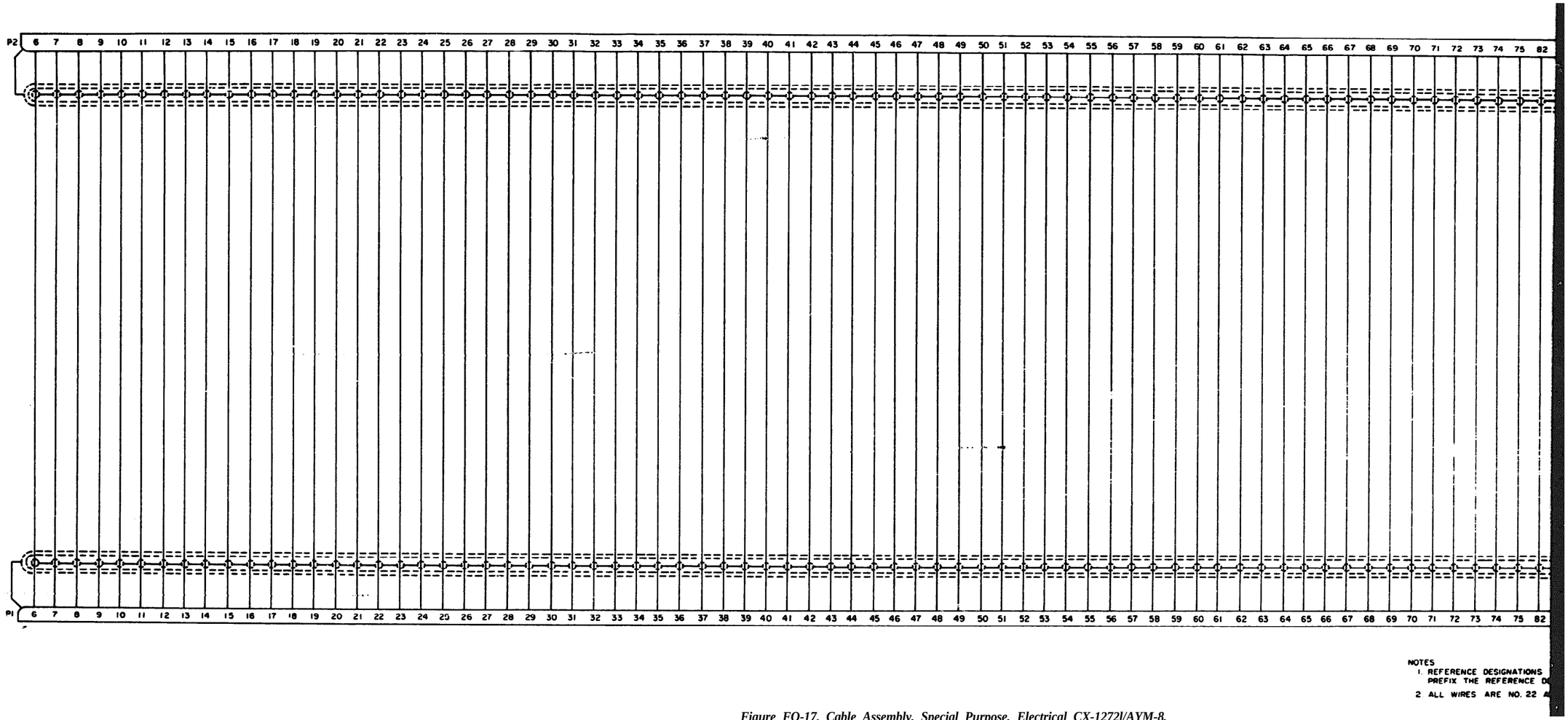


Figure FO-17. Cable Assembly, Special Purpose, Electrical CX-1272l/AYM-8, wiring diagram.

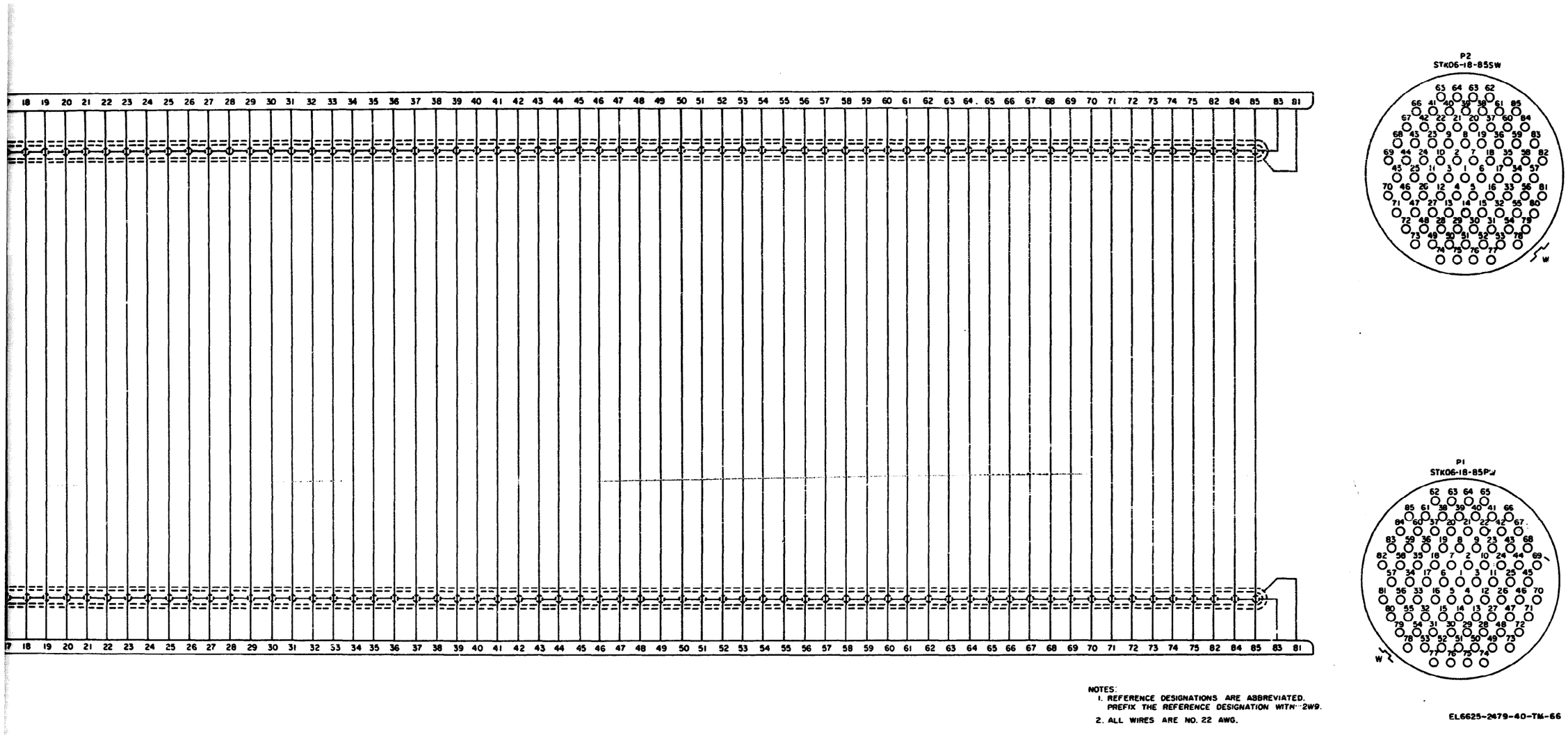
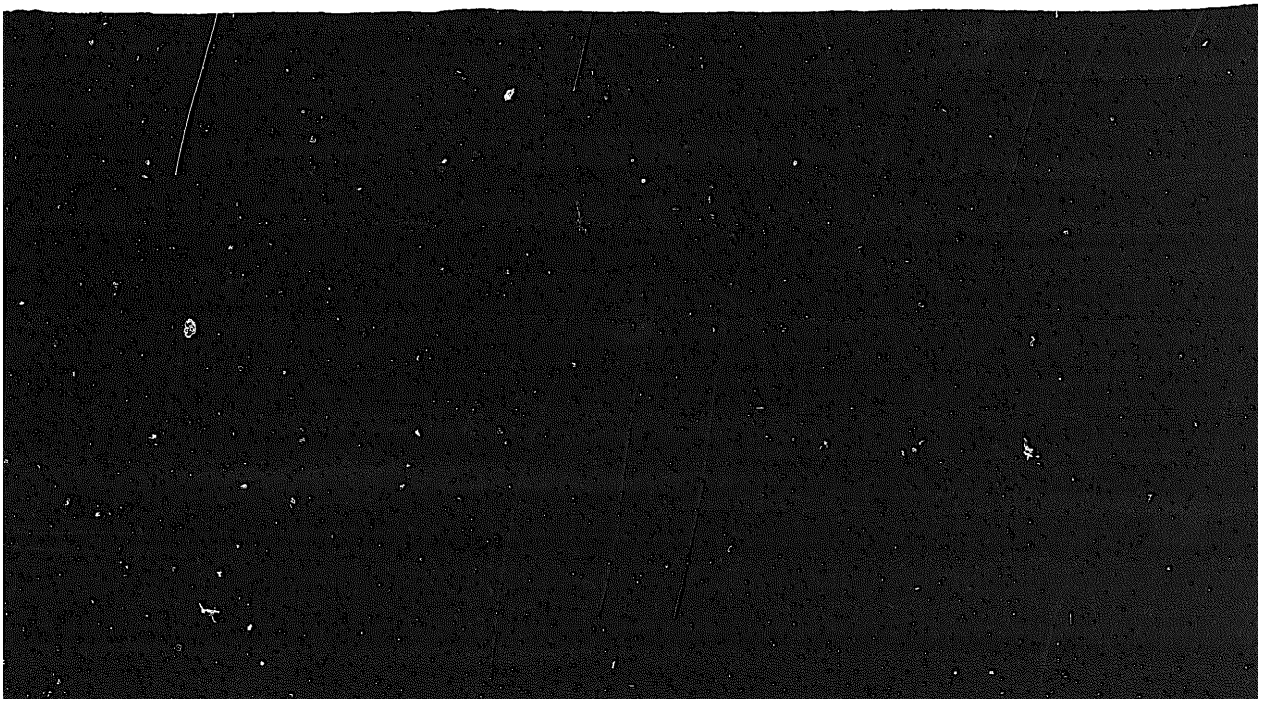


Figure FO-17. Cable Assembly, Special Purpose, Electrical CX-12721/AYM-8, *wiring diagram.*

END

12-25-82

DATE



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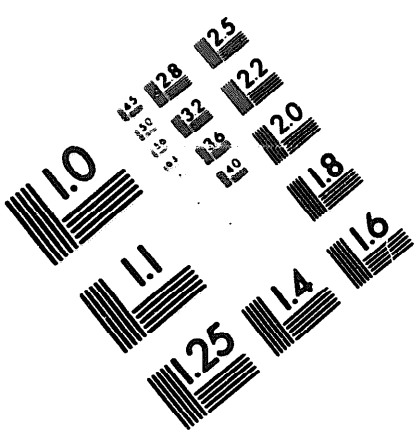
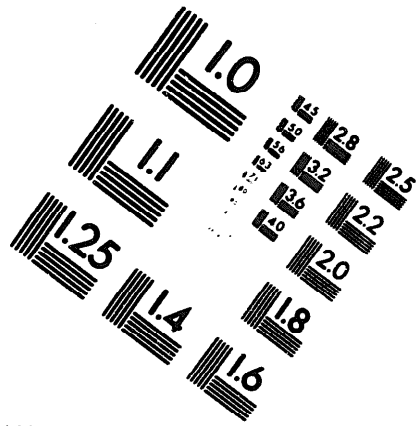
MICROFORM
TEST TARGET





150 MM

1.0 mm (e= 81 mm)

ABCDEFGHIJKLMNOPQRSTUVWXYZ1234567890
abcdefghijklmnopqrstuvwxyz$¢£/%#½¼¾—=+×&@*

1.5 mm (e= 1.09 mm)

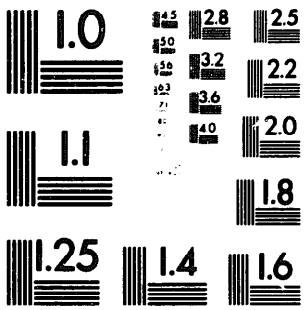
ABCDEFGHIJKLMNOPQRSTUVWXYZ1234567890
abcdefghijklmnopqrstuvwxyz$¢£/%#½¼¾—=+×&@*

2.0 mm (e= 1.37 mm)

ABCDEFGHIJKLMNOPQRSTUVWXYZ
abcdefghijklmnopqrstuvwxyz
1234567890$¢£/%#½¼¾—=+×&@*

2.5 mm (e= 1.77 mm)

ABCDEFGHIJKLMNOPQRSTUVWXYZ
abcdefghijklmnopqrstuvwxyz
1234567890$¢£/%#½¼¾—=+×&@*



1.0 mm (e= 81 mm)

ABCDEFGHIJKLMNOPQRSTUVWXYZ1234567890
abcdefghijklmnopqrstuvwxyz$¢£/%#½¼¾—=+×&@*

1.5 mm (e= 1.09 mm)

ABCDEFGHIJKLMNOPQRSTUVWXYZ1234567890
abcdefghijklmnopqrstuvwxyz$¢£/%#½¼¾—=+×&@*

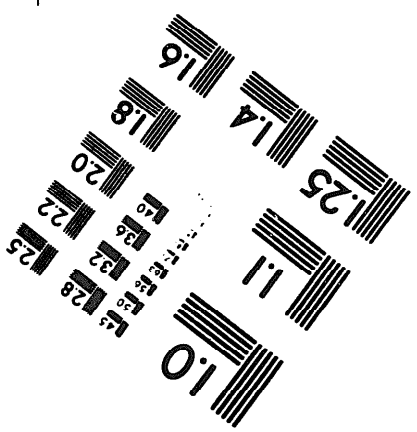
2.0 mm (e= 1.37 mm)

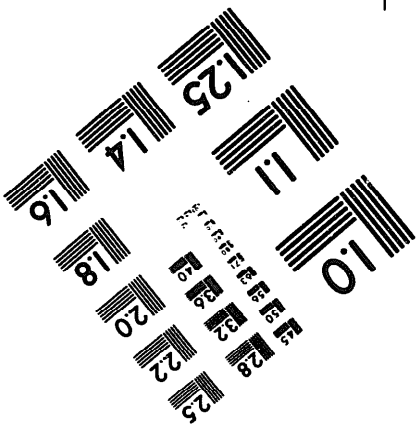
ABCDEFGHIJKLMNOPQRSTUVWXYZ
abcdefghijklmnopqrstuvwxyz
1234567890$¢£/%#½¼¾—=+×&@*

2.5 mm (e= 1.77 mm)

ABCDEFGHIJKLMNOPQRSTUVWXYZ
abcdefghijklmnopqrstuvwxyz
1234567890$¢£/%#½¼¾—=+×&@*

200 MM





250 MM